

648-M7

648FX-M7

661FX-M7


Rev: 1.2A


Revision History :

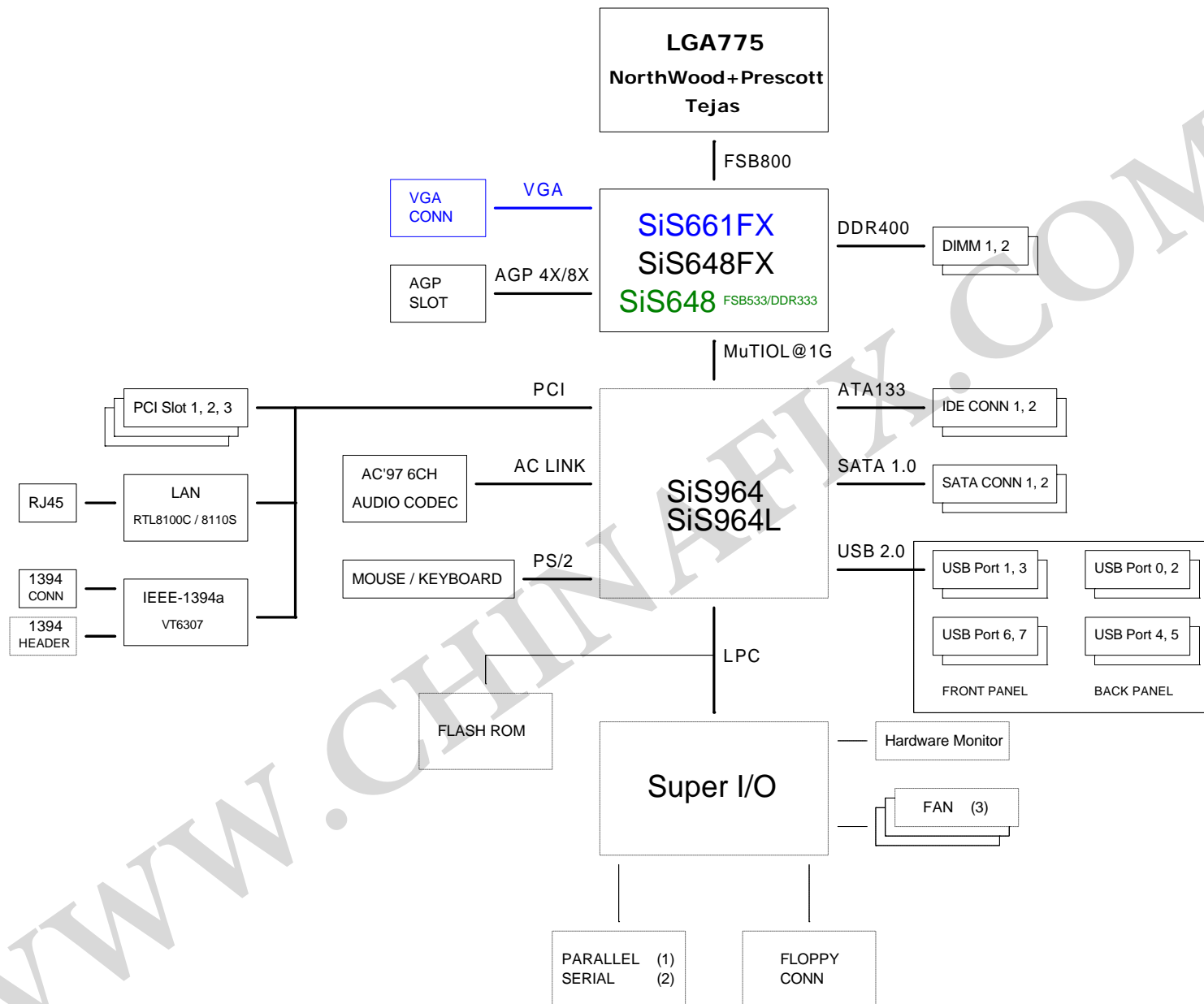
1. Ver A: Initial for 661FX/648FX for LGA775
2. Ver 1.0:
 - I. modify CPU pull-high
 - II. add FSB1066 select CKTs
 - III. modify Common-Choke and R0603 co-lay
 - IV. add 1394A3 header
 - V. AD1888 and ALC655 co-lay
 - VI. modify FAN CTRL CKTs
 - VII. modify VRDGD
 - VIII. add PANEL2
3. Ver 1.1:
 - I. modify for EE CPU supporting
 - II. modify SmartFAN clamp up circuit
4. Ver 1.1A:
 - I. modify for CPU 3pin SmartFAN supporting
 - II. Add SLVU2.8-4 Surge Protect IC
5. Ver 1.2A:
 - I. Add Dual core CPU Support
 - II. Removed AD1888 co-lay

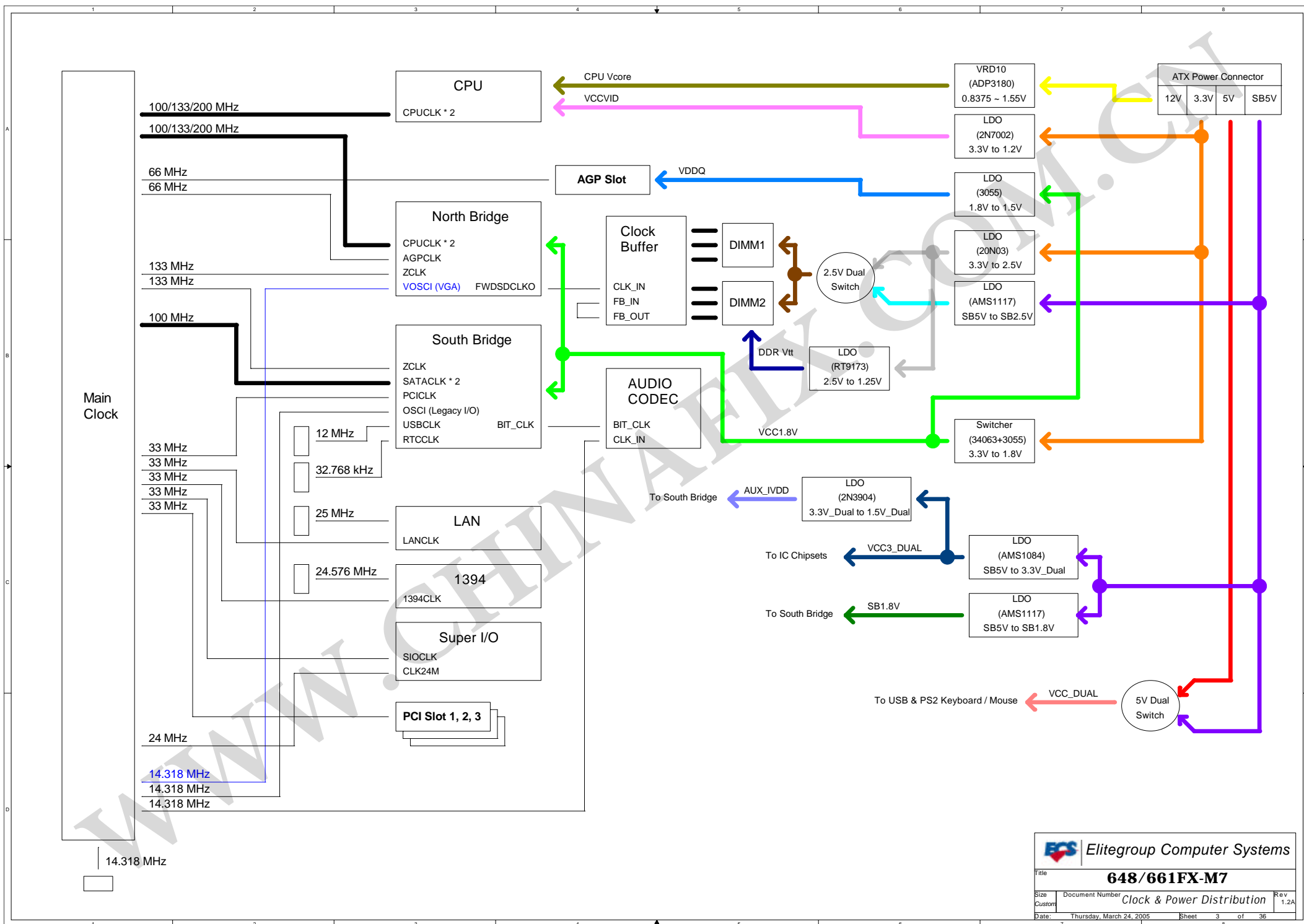
Page Index =====

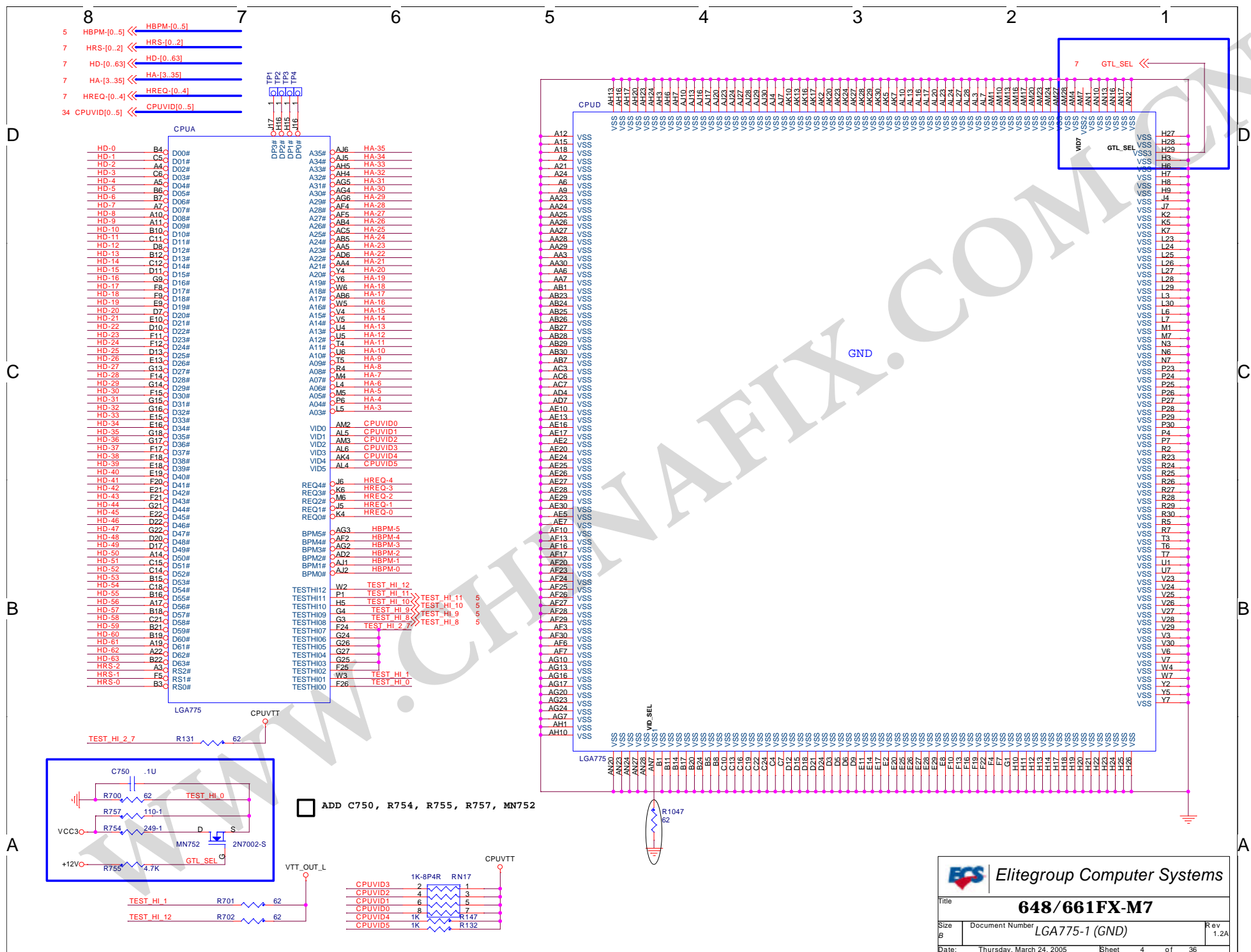
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|-------------------------------------|-------------------------------|
| 1. Cover Sheet | 21. USB Connector |
| 2. Block Diagram | 22. PCI Slot1, 2 |
| 3. Clock & Power Distribution | 23. PCI Slot3 / LANPHY |
| 4. Socket LGA775-1 | 24. LAN |
| 5. Socket LGA775-2 | 25. IEEE1394a |
| 6. Socket LGA775-3 | 26. Audio Codec |
| 7. SiS661FX-1 (HOST / AGP) | 27. Audio Interface |
| 8. SiS661FX-2 (Memory) | 28. Super I/O |
| 9. SiS661FX-3 (VGA / HyperZip) | 29. KB/MS/ROM/FDC/IR |
| 10. SiS661FX-4 (Power) | 30. COM 1,2 / LPT |
| 11. SiS964-1 (PCI / IDE / HyperZip) | 31. HM/FAN/RING/LPC |
| 12. SiS964-2 (Misc. Signals) | 32. Voltage Regulator |
| 13. SiS964-3 (USB) | 33. DUAL 5V, 3V& SB Regulator |
| 14. SiS964-4 (Power) | 34. VRD10 (CPU Vcore) |
| 15. Main Clock | 35. ATX / Panel / RTC |
| 16. Clock Buffer | 36. BOM and GPIO Attention |
| 17. DDR DIMM 1, 2 | |
| 18. DDR Termination | |
| 19. AGP slot | |
| 20. VGA / IDE Connectors | |

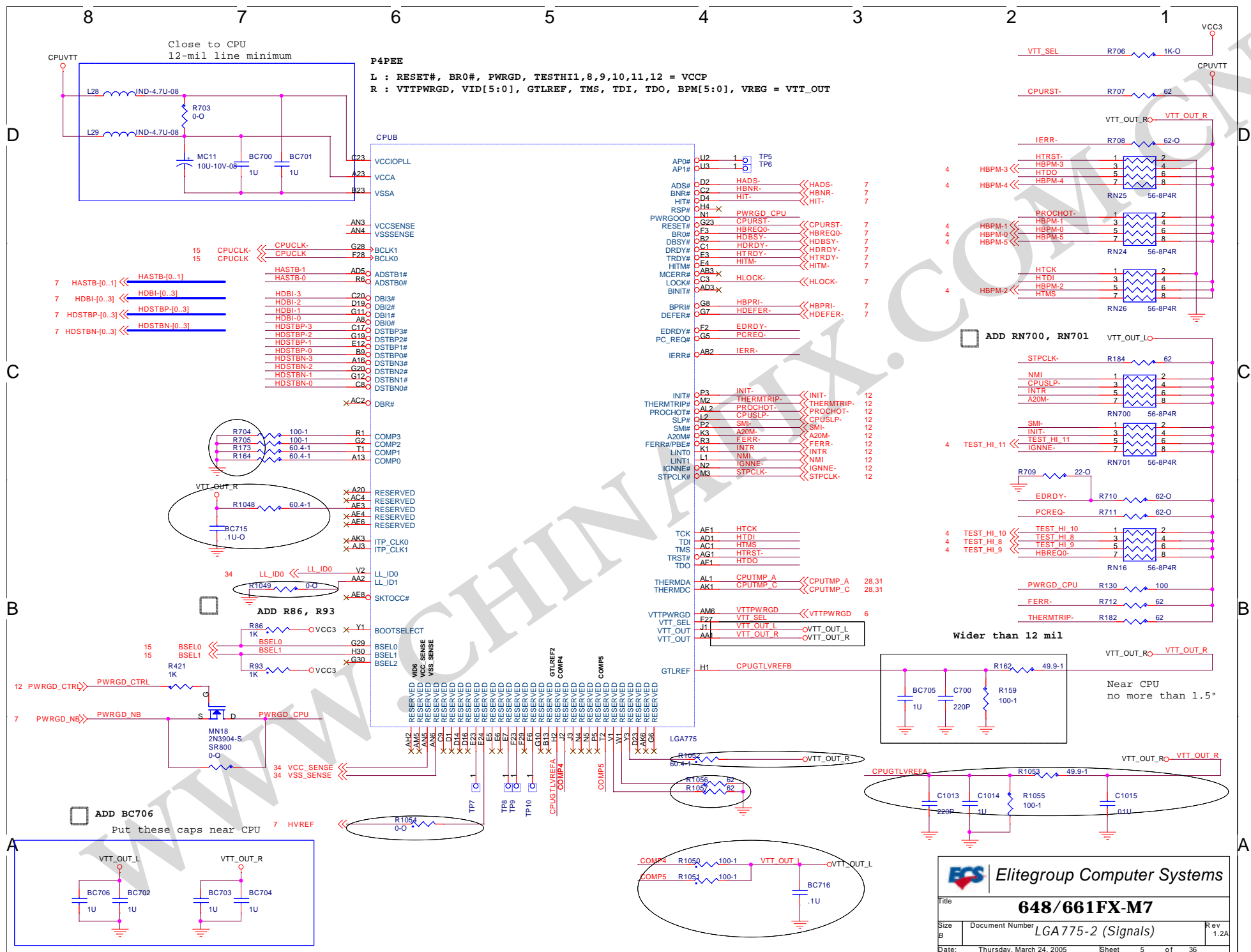
 SIGNATURE	DATE
DESIGNER Prowind	
LAYOUT ECS Layout team	
CHECK Prowind	
APPROVAL	

 Elitegroup Computer Systems	
Title 648/661FX-M7	
Size Custom	Document Number Cover Sheet
Date: Thursday, March 24, 2006	Sheet 1 of 36
	Rev 1.2A



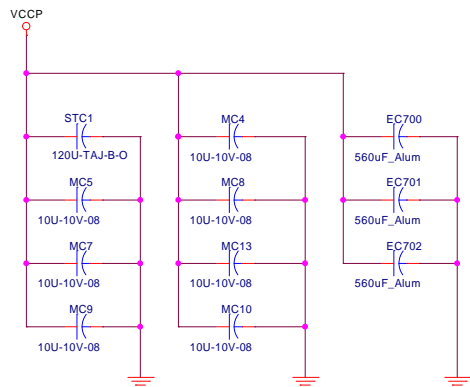




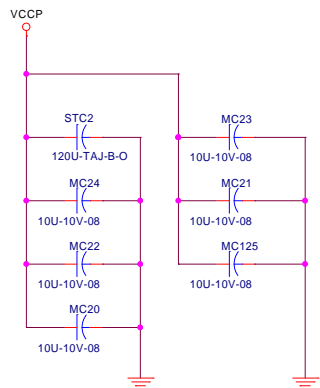


P.S. Choose X5R components instead of Y5V for all 22uF_1206 capacitors on this page.

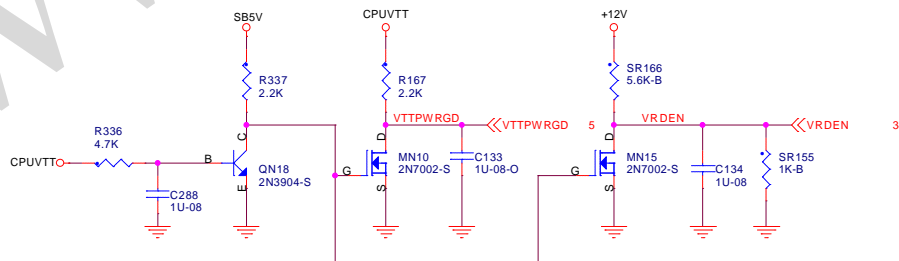
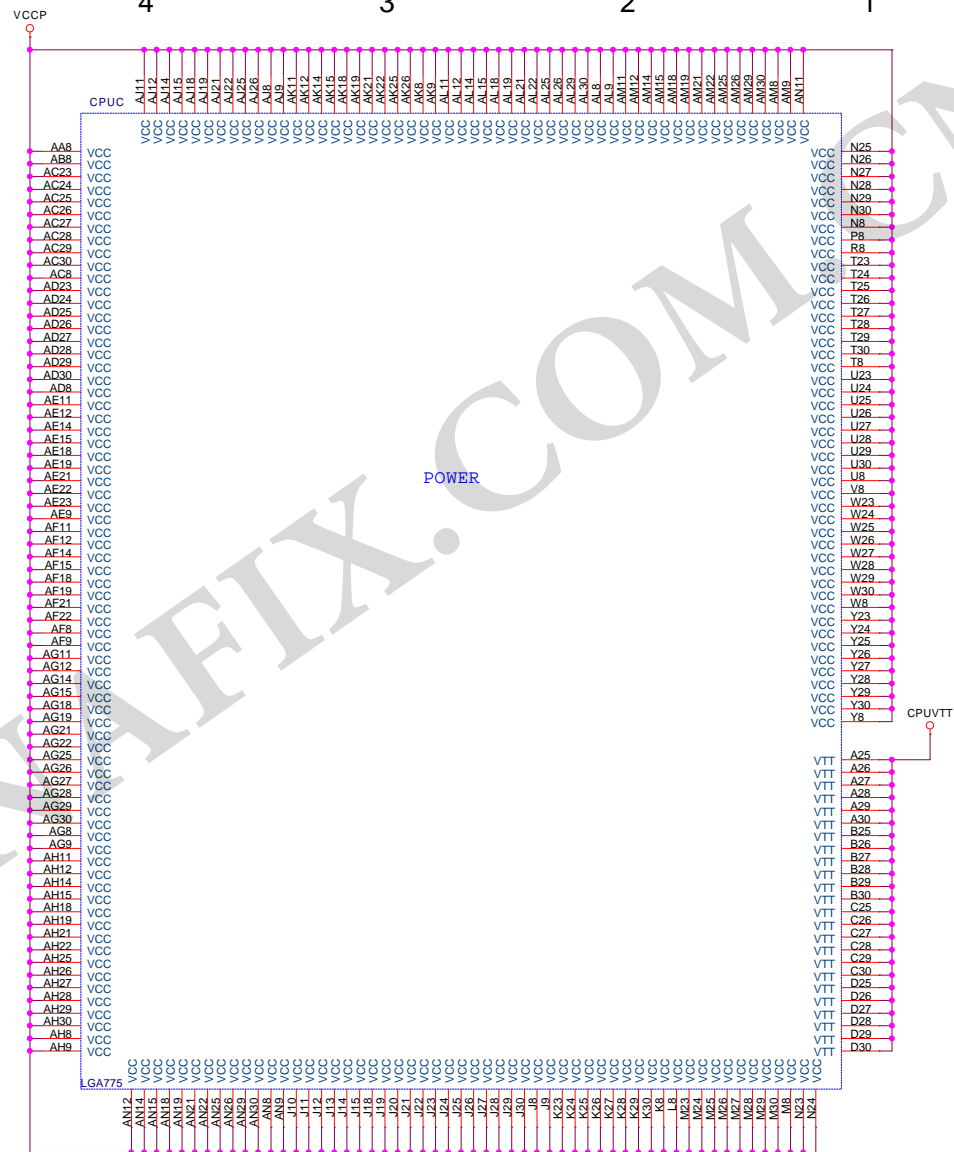
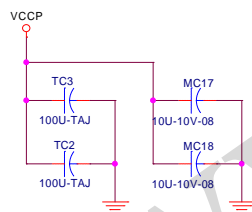
Put these capacitors at processor TOP SIDE



Put these capacitors at processor LEFT SIDE



Put these capacitors INSIDE PROCESSOR CAVITY



U8B

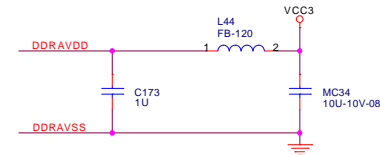
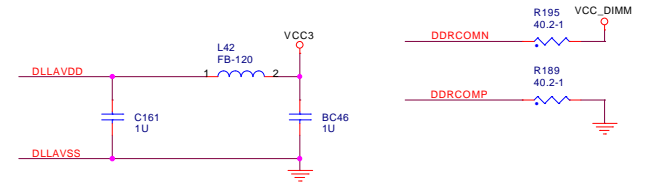
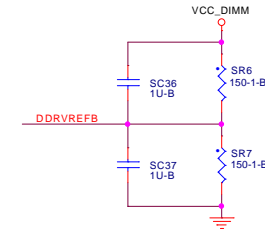
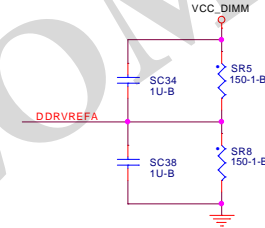
661FX-2

DMD0	AN35	MD0
DMD1	AP36	MD1
DMD2	AK33	MD2
DMD3	AM33	MD3
DMD4	AN34	MD4
DMD5	AK32	MD5
DMD6	AR34	MD6
DMD7	AN33	MD7
DDQM0	AR36	DOM0
DDQS0	AP34	DQS0/CSB0#
DMD8	AM32	MD8
DMD9	AL31	MD9
DMD10	AR31	MD10
DMD11	AL30	MD11
DMD12	AN32	MD12
DMD13	AR33	MD13
DMD14	AN31	MD14
DMD15	AM31	MD15
DDQM1	AR32	DQM1
DDQS1	AP32	DQS1/CSB1#
DMD16	AP30	MD16
DMD17	AR30	MD17
DMD18	AN29	MD18
DMD19	AL27	MD19
DMD20	AN30	MD20
DMD21	AN28	MD21
DMD22	AL28	MD22
DMD23	AN28	MD23
DDQM2	AL29	DOM2
DDQS2	AP28	DQS2/CSB2#
DMD24	AP28	MD24
DMD25	AN25	MD25
DMD26	AR24	MD26
DMD27	AL24	MD27
DMD28	AL25	MD28
DMD29	AR26	MD29
DMD30	AM25	MD30
DMD31	AN24	MD31
DDQM3	AP24	DQM3
DDQS3	AR25	DQS3/CSB3#
DMD32	AN21	MD32
DMD33	AP20	MD33
DMD34	AN20	MD34
DMD35	AL18	MD35
DMD36	AM21	MD36
DMD37	AR21	MD37
DMD38	AL19	MD38
DMD39	AM19	MD39
DDQM4	AR20	DOM4
DDQS4	AP20	DQS4/CSB4#
DMD40	AL15	MD40
DMD41	AL14	MD41
DMD42	AN15	MD42
DMD43	AR15	MD43
DMD44	AN16	MD44
DMD45	AM15	MD45
DMD46	AL14	MD46
DMD47	AL13	MD47
DDQM5	AP16	DOM5
DDQS5	AR16	DQS5/CSB5#
DMD48	AM13	MD48
DMD49	AL12	MD49
DMD50	AL11	MD50
DMD51	AR12	MD51
DMD52	AP14	MD52
DMD53	AR14	MD53
DMD54	AN13	MD54
DMD55	AP12	MD55
DDQM6	AN12	DOM6
DDQS6	AR13	DQS6/CSB6#
DMD56	AL10	MD56
DMD57	AR11	MD57
DMD58	AM9	MD58
DMD59	AR9	MD59
DMD60	AM11	MD60
DMD61	AN11	MD61
DMD62	AP10	MD62
DMD63	AN9	MD63
DDQM7	AN10	DOM7
DDQS7	AR10	DQS7/CSB7#

SIS661FX

MA0	AR23	DMA0
MA1	AN22	DMA1
MA2	AM23	DMA2
MA3	AL23	DMA3
MA5	AL26	DMA5
MA6	AN26	DMA6
MA7	AN27	DMA7
MA8	AR27	DMA8
MA9	AR28	DMA9
MA10	AP22	DMA10
MA11	AN18	DMA11
MA12	AR22	DMA12
MA13	AP28	DMA13
MA14	AM27	DMA14
MA15	AT14	
SRAS#	AL17	DRAS-
SCAS#	AR19	DCAS-
SWE#	AN19	DWE-
CS0#	AM17	DCS-0
CS1#	AL16	DCS-1
CS2#	AN17	DCS-2
CS3#	AR17	DCS-3
CS4#	AP18	
CS5#	AR18	
CKE0	AP4	CKE0
CKE1	AT3	CKE1
CKE2	AR3	CKE2
CKE3	AP3	CKE3
CKE4	AR2	
CKE5	AN4	
S3AUXSW#	AP2	S3AUXSW-
FWDSCLK0	AL21	FWDSCLK0
DRAMTEST	AL22	
10.15mA DLLAVDD	AL35	DLLAVDD
DLLAVSS	AL34	DLLAVSS
24.86mA DDRAVDD	AM35	DDRAVDD
DDRAVSS	AN36	DDRAVSS
DDRVREFB	AF16	DDRVREFB
DDRVREFA	AF23	DDRVREFA
TRAP2	AP1	
DDRCOMP_P	AR8	DDRCOMP
DDRCOMP_N	AP8	DDRCOMP

DMD[0..63]	DDMD[0..63]	17,18
DDQM[0..7]	DDQM[0..7]	17,18
DDQS[0..7]	DDQS[0..7]	17,18
DMA[0..14]	DMA[0..14]	17,18
DCS-[0..3]	DCS-[0..3]	17,18
CKE[0..3]	CKE[0..3]	17



Elitegroup Computer Systems

Title			648/661FX-M7
Size	Document Number	SiS661FX-2 (Memory)	
Custom			Rev 1.2A
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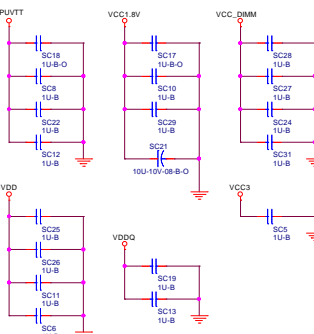
661FX-4

Power

NOTE:
SiS648FX doesn't have
the following 9 balls:
VDDQ(P12), VDDQ(AE14), VDDQ(AE15),
VDDQ(AB25), IVDD(N20), IVDD(T24),
VTT(M20), VTT(N25), VTT(P25).

AUX_IVDD=10.12mA
AUX3.3=26.38mA

Place these capacitors under 648 solder side



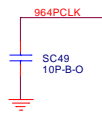
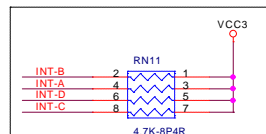
But SiS648 and SiS660 still
have these 9 balls.

Elitegroup Computer Systems

648/661FX-M7

Document Number: SiS661FX-4 (Power)

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22,23,24,25 CBE-[0..3] << CBE-[0..3]

9,19,22,23,24,25 INT-A << INT-A
19,22,23,25 INT-B << INT-B
22,23,24 INT-C << INT-C
22,23 INT-D << INT-D

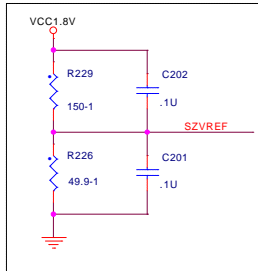
22,23,24,25 FRAME- << FRAME-
22,23,24,25 IRDY- << IRDY-
22,23,24,25 TRDY- << TRDY-
22,23,24,25 STOP- << STOP-

22,23,24 SERR- << SERR-
22,23,24,25 PAR << PAR
22,23,24,25 DEVSEL- << DEVSEL-
22,23 PLOCK- << PLOCK-

15 964PCLK << 964PCLK
19,20,22,23,24,25,29 PCIRST- << PCIRST-
28 SIOPCIRST- << SIOPCIRST-
9 NBPCIRST- << NBPCIRST-

15 964ZCLK << 964ZCLK
9 ZSTB0 << ZSTB0
9 ZSTB-0 << ZSTB-0
9 ZSTB1 << ZSTB1
9 ZSTB-1 << ZSTB-1

9 ZUREQ << ZUREQ
9 ZDREQ << ZDREQ



SZCMP_N AA24 ZCMP_N

SZCMP_P AA25 ZCMP_P

SZ1XAVDD AC26 Z1XAVDD 12mA

SZ1XAVSS AB25 Z1XAVSS

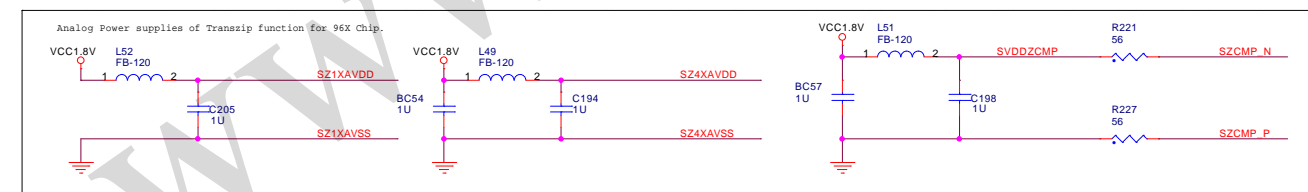
SZ4XAVDD Y22 Z4XAVDD 34mA

SZ4XAVSS AA23 Z4XAVSS

SZVREF AA26 ZVREF

ZAD16 Y26 ZAD16

9 ZADJ[0..16] << ZADJ[0..16]



PCI

IDE

964-1

HyperZip

Programmable on-die pull-high strength for CPU_S:
(Infinite, 150, 110, 56 Ohm)

U13B

CPU_S

APIC

LPC

RTC

964-2

GPIO

AC97

ACPI
/others

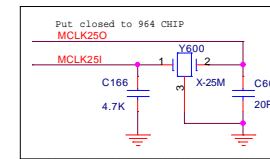
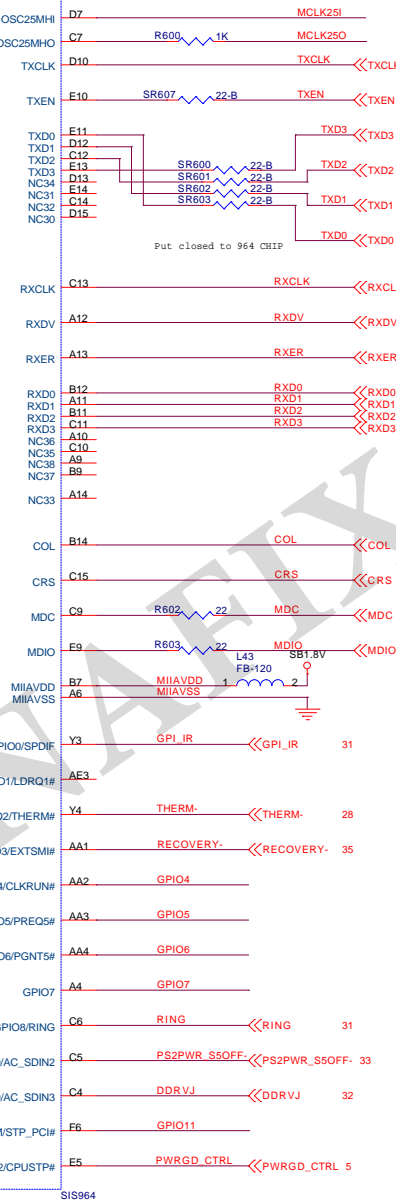
GPIO

KBC

/geyserville

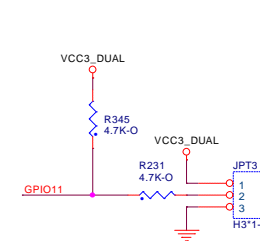
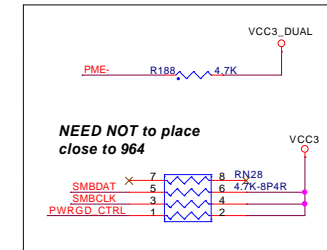
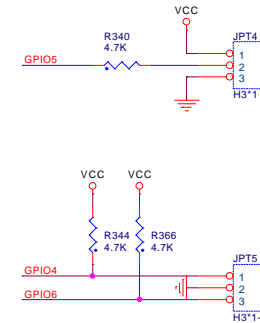
MII

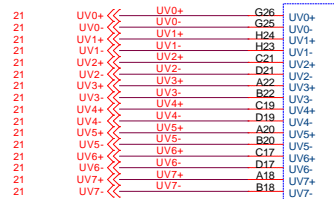
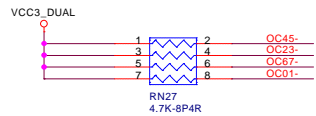
SiS963, 964 GPIO 0-7
internal pull up
SiS963, 964 GPIO 9,10
internal pull down



	SB GPIO	Function	High(1-2)	Low(2-3)
JPT4	GPI5	Suspend Mode	S1 & S3	S1 only
	GPI7	LAN Select	PCILAN	LANPHY
	GPO9	S5 Wake-up	Enable	Disable
JPT3	GPI11	CPU Select	04B/FMB1.5	04A/FMB1.0
	GPIO12	CPUPWRGD_CTRL	By SiS Programming Guide	
	GPO13	Flash EN-	Write Enable	Write Disable
	GPO2	ThermWarming-	Normal	OverTemp

	SIO GPIO	Function	High	Low
	GPO47	FAN_ON-	LowSpeed	HighSpeed
	GPO62	ROM_TBL-	Write Enable	Protect
	GPI66	ThermWarming-	Normal	OverTemp
	GPO67	OverTempBeep	Beep	Normal



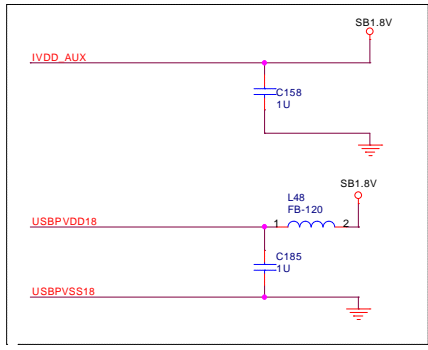
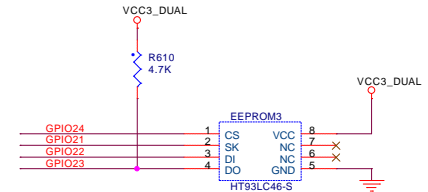
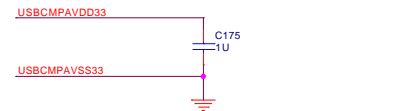
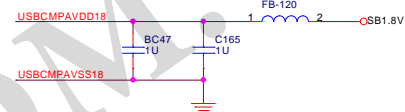
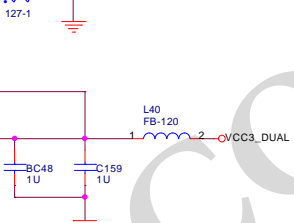
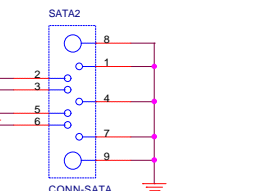
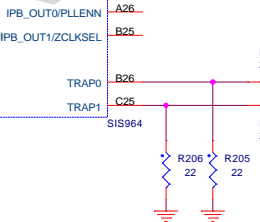
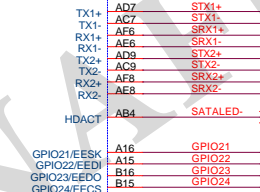
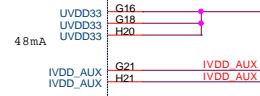
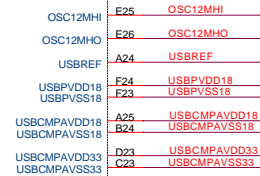
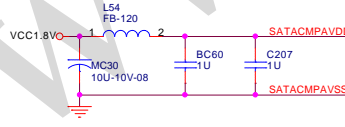
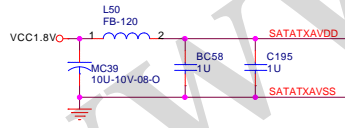
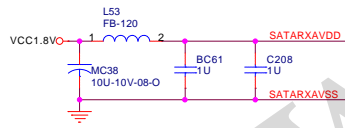
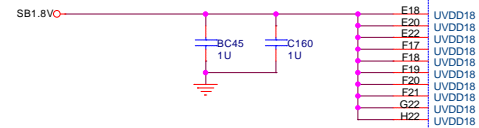


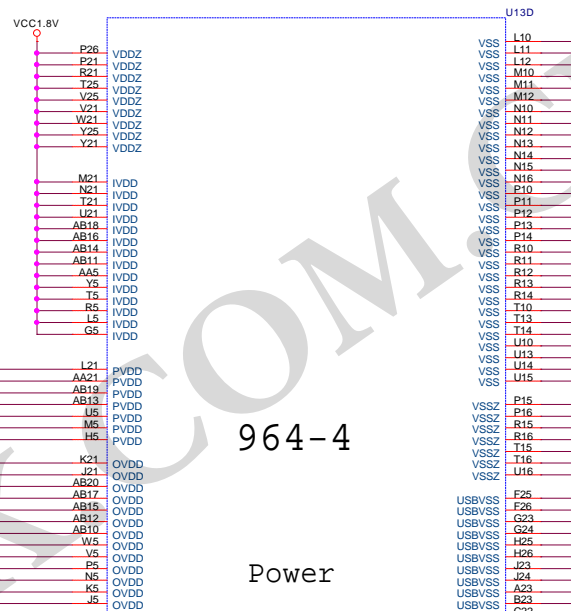
U13C

USB

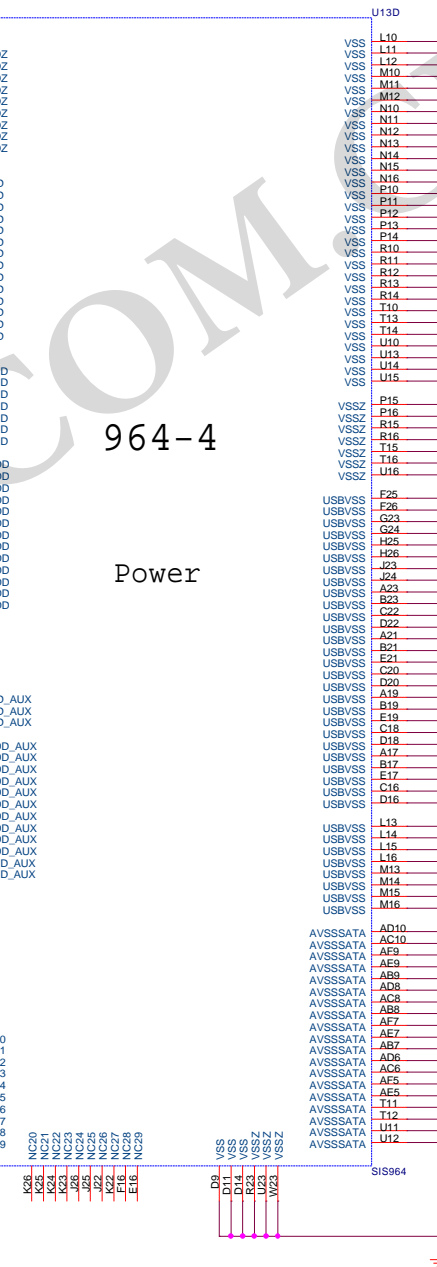
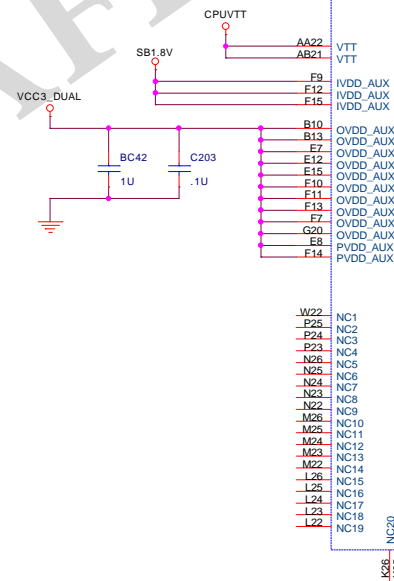
330mA

964-3

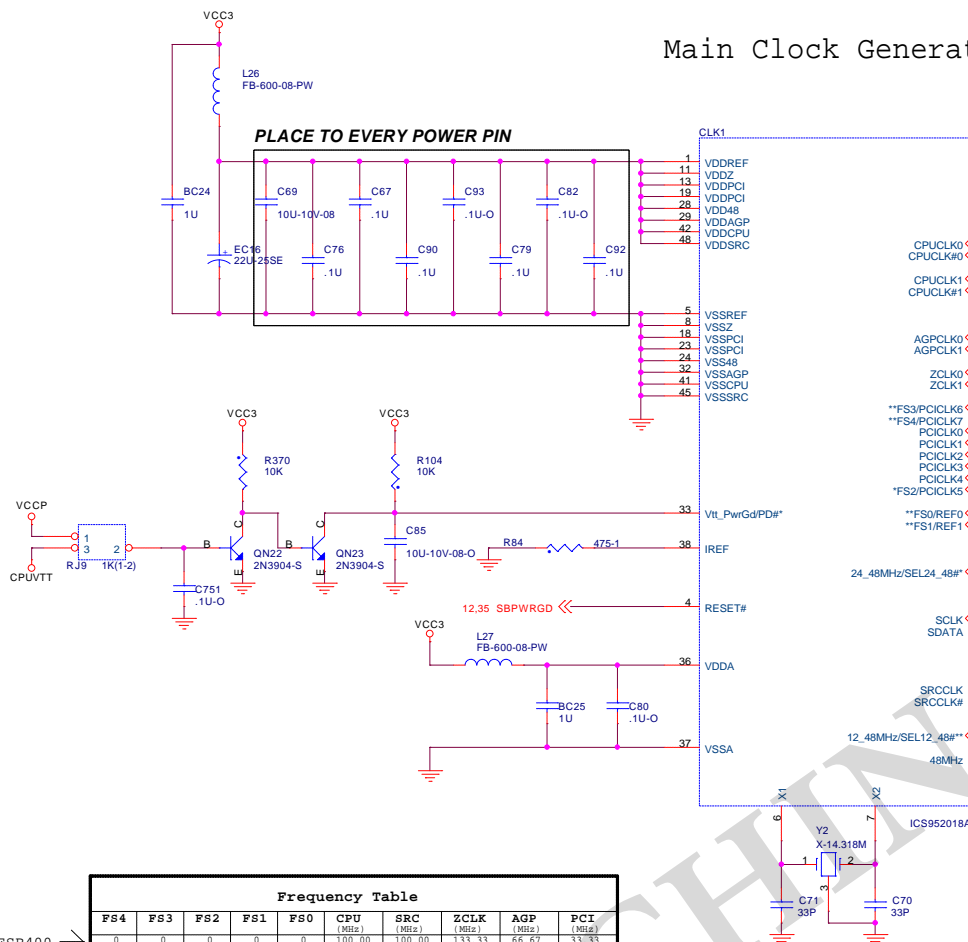




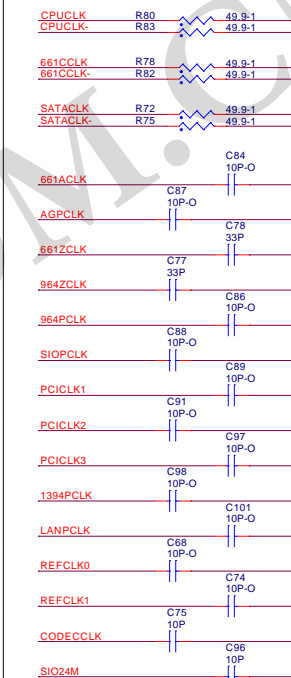
Power



Main Clock Generator



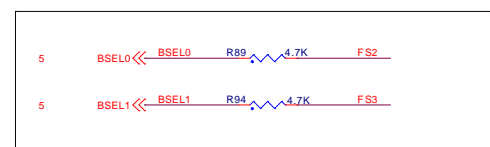
By-Pass Capacitors
Place near to the Clock Outputs



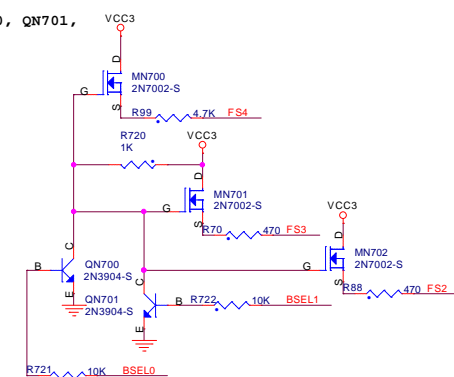
Frequency Table									
FS4	FS3	FS2	FS1	FS0	CPU (Hz)	SRC (Hz)	ZCLK (Hz)	AGP (Hz)	PCI (Hz)
0	0	0	0	0	100.00	100.00	133.33	66.67	33.33
0	0	0	0	1	100.99	100.99	134.65	67.33	33.66
0	0	0	1	0	103.00	103.00	137.33	68.67	34.33
0	0	0	1	1	103.99	103.99	138.33	69.33	35.33
0	0	1	0	0	133.33	100.00	133.33	66.66	33.33
0	0	1	0	1	134.65	100.99	134.65	67.32	33.66
0	0	1	1	0	137.33	103.00	137.33	68.66	34.33
0	0	1	1	1	138.33	103.99	138.33	69.33	35.33
0	1	0	0	0	200.00	100.00	133.33	66.67	33.33
0	1	0	0	1	201.98	100.99	134.65	67.33	33.66
0	1	0	1	0	206.00	103.00	137.33	68.67	34.33
0	1	0	1	1	208.00	103.99	138.33	69.33	35.33
0	1	1	0	0	166.66	125.00	125.00	66.66	33.33
0	1	1	0	1	168.31	126.23	126.23	67.32	33.66
0	1	1	1	0	171.66	128.74	128.74	68.66	34.33
0	1	1	1	1	174.66	131.25	131.25	69.66	35.33

Frequency Table									
FS4	FS3	FS2	FS1	FS0	CPU (Hz)	SRC (Hz)	ZCLK (Hz)	AGP (Hz)	PCI (Hz)
1	0	0	0	0	105.00	105.00	140.00	70.00	35.00
1	0	0	0	1	107.00	107.00	142.00	71.33	35.67
1	0	0	1	0	109.00	109.00	145.33	72.67	36.33
1	0	1	0	0	110.00	110.00	146.67	73.33	36.67
1	0	1	0	1	140.00	105.00	140.00	70.00	35.00
1	0	1	0	1	142.66	107.00	142.67	71.33	35.67
1	0	1	1	0	145.33	109.00	145.33	72.66	36.33
1	0	1	1	1	146.66	110.00	146.66	73.33	36.67
1	1	0	0	0	210.00	105.00	140.00	70.00	35.00
1	1	0	0	1	214.00	107.00	142.67	71.33	35.67
1	1	0	1	0	218.00	109.00	145.33	72.67	36.33
1	1	0	1	1	220.00	110.00	146.67	73.33	36.67
1	1	1	0	0	266.66	100.00	133.33	66.67	33.33
1	1	1	0	1	269.33	101.00	134.67	67.33	33.67
1	1	1	1	0	274.66	103.00	137.33	68.67	34.33
1	1	1	1	1	266.66	100.00	133.33	66.67	33.33

Frequency Selection



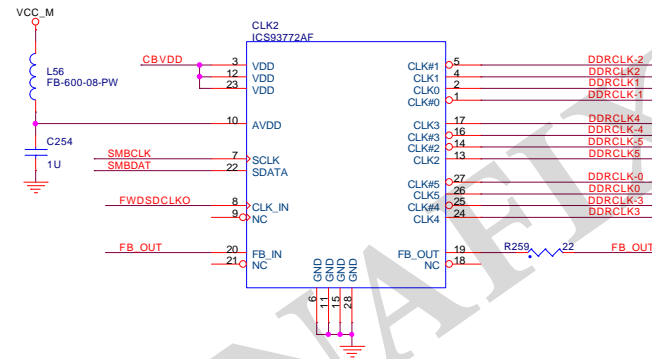
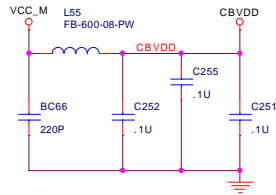
<i>Clock Generator Table</i>	<i>FS4</i>	<i>FS3</i>	<i>FS2</i>	<i>FS1</i>	<i>FS0</i>
<i>Hardware Trapping</i>	<i>Low</i>	<i>Low</i>	<i>BSEL2</i>	<i>BSEL1</i>	<i>BSEL</i>
<i>CPU=100 (BSEL[2:0]=101)</i>					
<i>CPU=133 (BSEL[2:0]=001)</i>	<i>0</i>	<i>0</i>	<i>1</i>	<i>0</i>	<i>0</i>
<i>CPU=166 (BSEL[2:0]=011)</i>	<i>0</i>	<i>1</i>	<i>1</i>	<i>0</i>	<i>0</i>
<i>CPU=200 (BSEL[2:0]=010)</i>	<i>0</i>	<i>1</i>	<i>0</i>	<i>0</i>	<i>0</i>
<i>CPU=266 (BSEL[2:0]=000)</i>	<i>1</i>	<i>1</i>	<i>1</i>	<i>0</i>	<i>0</i>



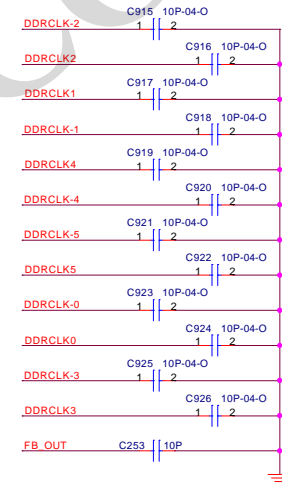
Clock Buffer (DDR)

(5 OPTIONS)
 1: (ICS) ICS93716
 2: (Winbond)
 3: (ICWorks)
 4: (IMI)
 5: (AMI)

By-Pass Capacitors
 Place near to the Clock Buffer

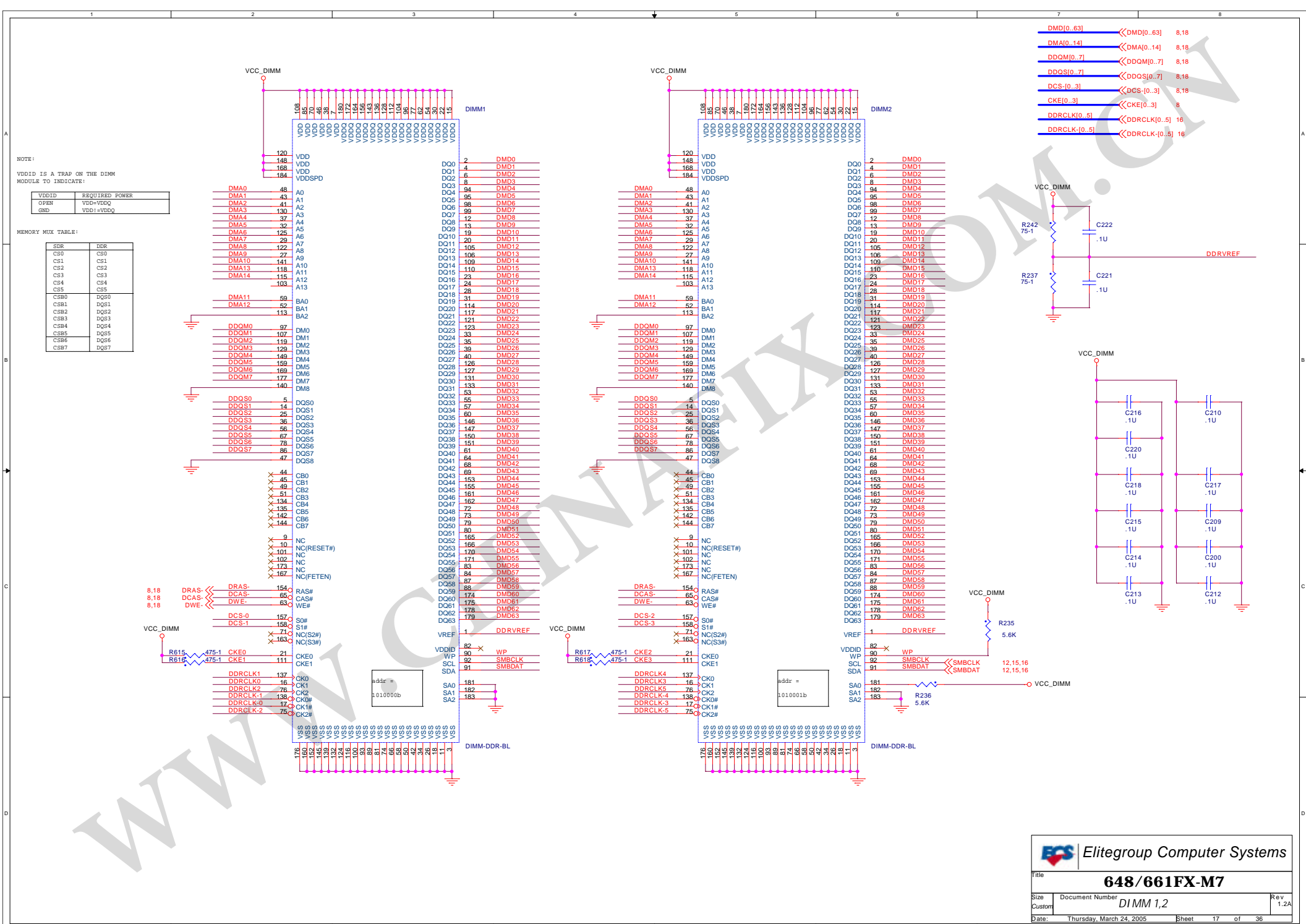


DDRCLK[0..5] <<DDRCLK[0..5] 17
 DDRCLK[10..5] <<DDRCLK[10..5] 17
 SMBCLK <<SMBCLK 12,15,17
 SMBDAT <<SMBDAT 12,15,17
 FWDSDCLKO <<FWDSDCLKO 8



Elitegroup Computer Systems

Title		648/661FX-M7	
Size	Document Number	Clock Buffer	
Custom		Rev 1.2A	
Date:	Thursday, March 24, 2005	Sheet 16	of 36



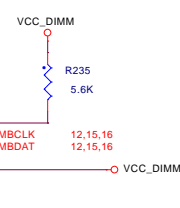
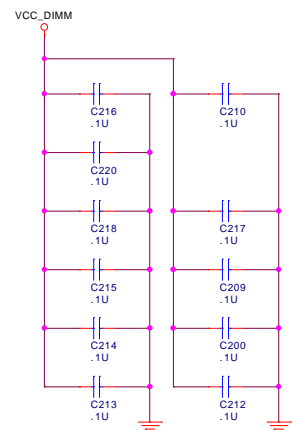
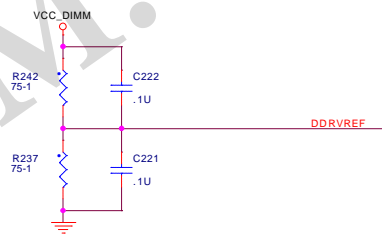
NOTE:
VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD1=VDDQ

MEMORY MIX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CS6	CS6
CS7	CS7

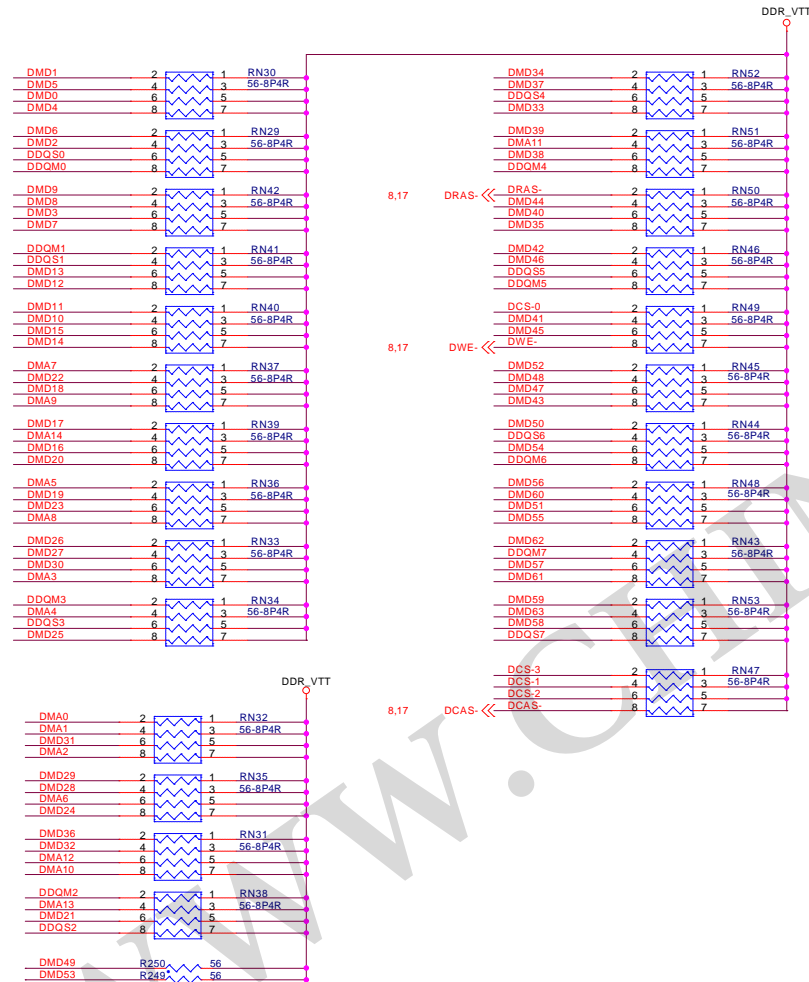
- DMD[0..63] << DMD[0..63] 8,18
- DMA[0..14] << DMA[0..14] 8,18
- DDQM[0..7] << DDQM[0..7] 8,18
- DDQS[0..7] << DDQS[0..7] 8,18
- DCS[0..3] << DCS[0..3] 8,18
- CKE[0..3] << CKE[0..3] 8
- DDRCLK[0..5] << DDRCLK[0..5] 16
- DDRCLK[0..5] << DDRCLK[0..5] 16



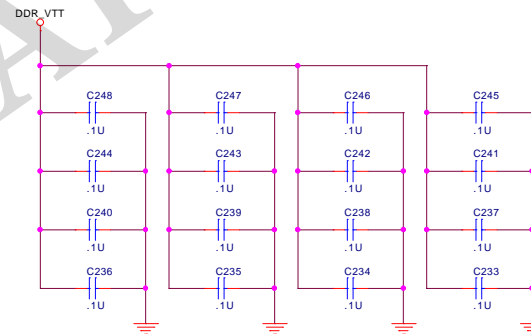
SSTL-2 Termination Resistors

	SDR		DDR		
MD/DQM (/DQS)	I/V-CMOS	R _s	SSTL-2	R _s	R _{tt}
MA/Control	I/V-CMOS	0/10/-	SSTL-2	10	33
CS	I/V-CMOS	0	SSTL-2	0	33
CKE	DD 3.3V		DD 2.5V		47

DMD[0..63]	8.17
DMA[0..14]	8.17
DDQM[0..7]	8.17
DDQS[0..7]	8.17
DCS[0..3]	8.17

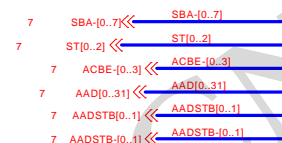


DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs

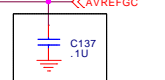


Elitegroup Computer Systems

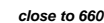
Title	648/661FX-M7		
Size	Document Number	DDR Termination	Rev 1.2A
Custom			
Date:	Thursday, March 24, 2005	Sheet 18 of 36	

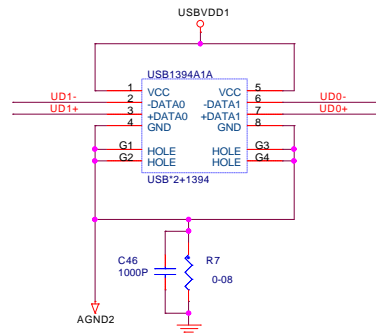
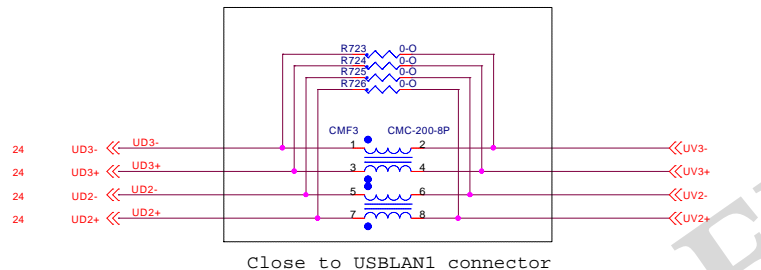
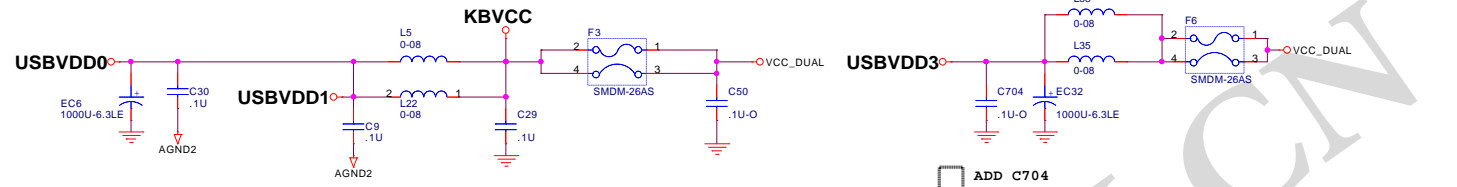
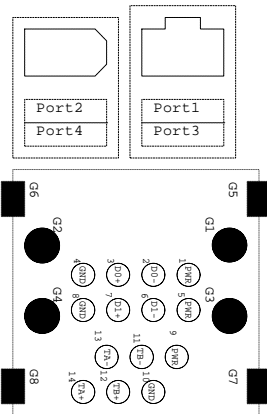


GCDET-	Low	Hi
Graphic Card	AGP 3.0	AGP 2
AVREFCG	0.35	0.75
APERR	0	1.5



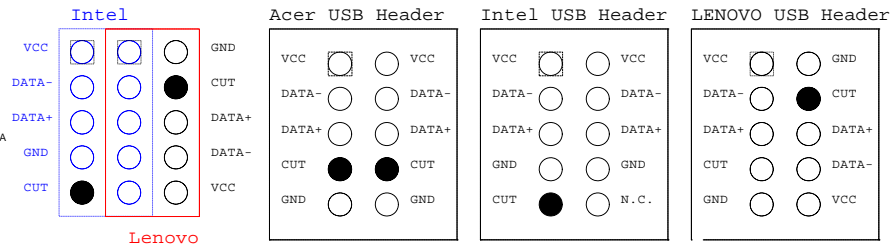
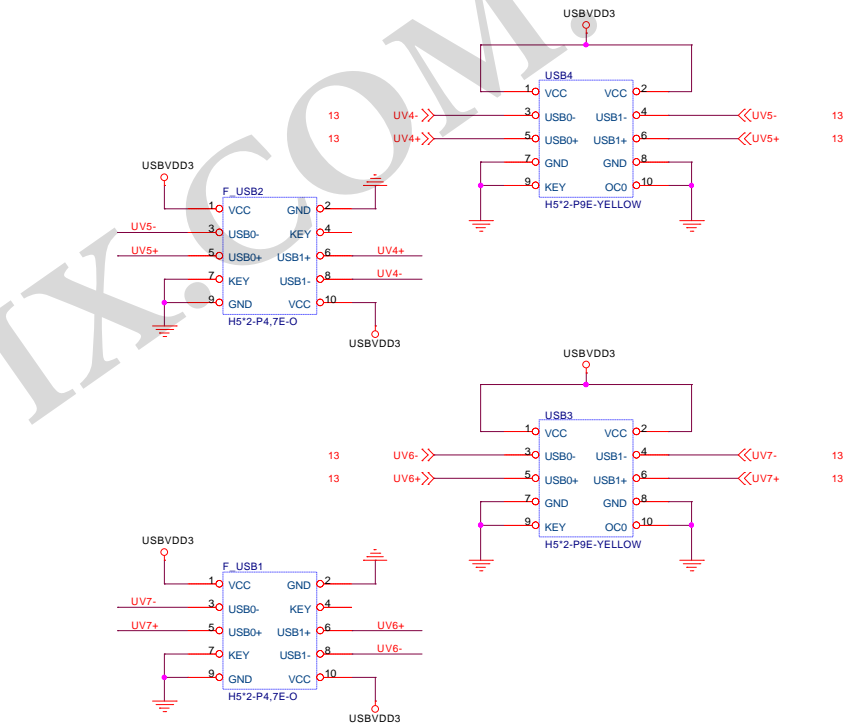
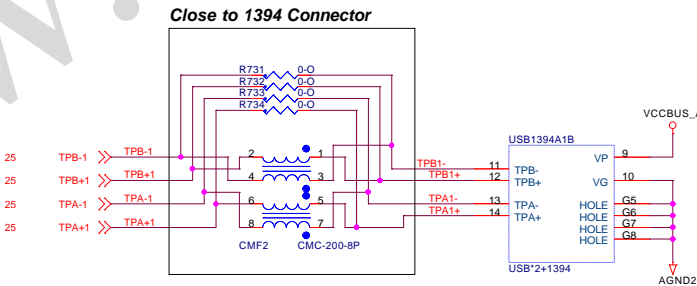
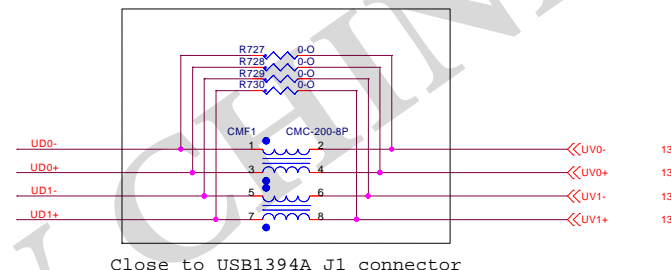
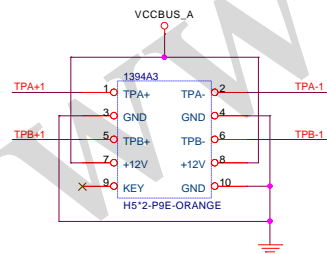
put CAP close to AGP slot each POWER PIN



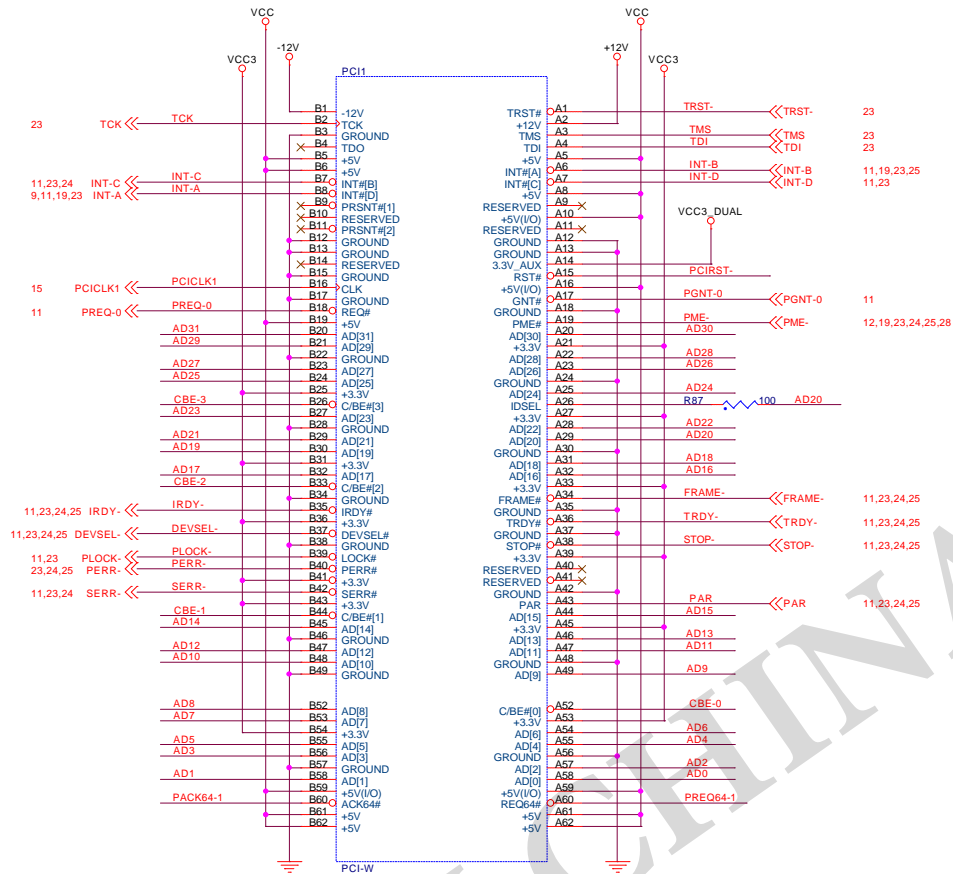


	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5

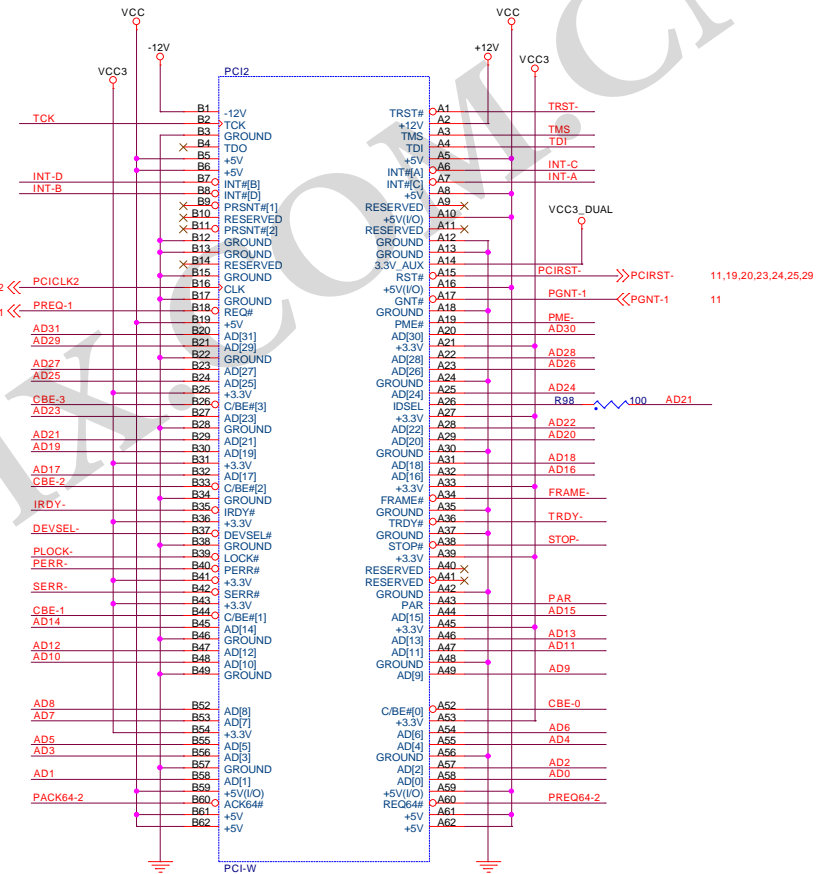
ADD 1394A3



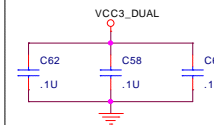
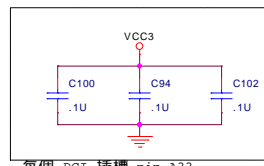
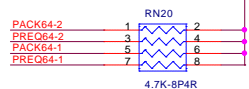
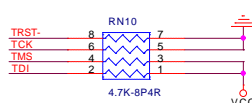
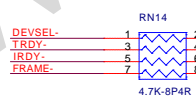
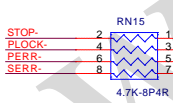
PCI Slot 1 & 2



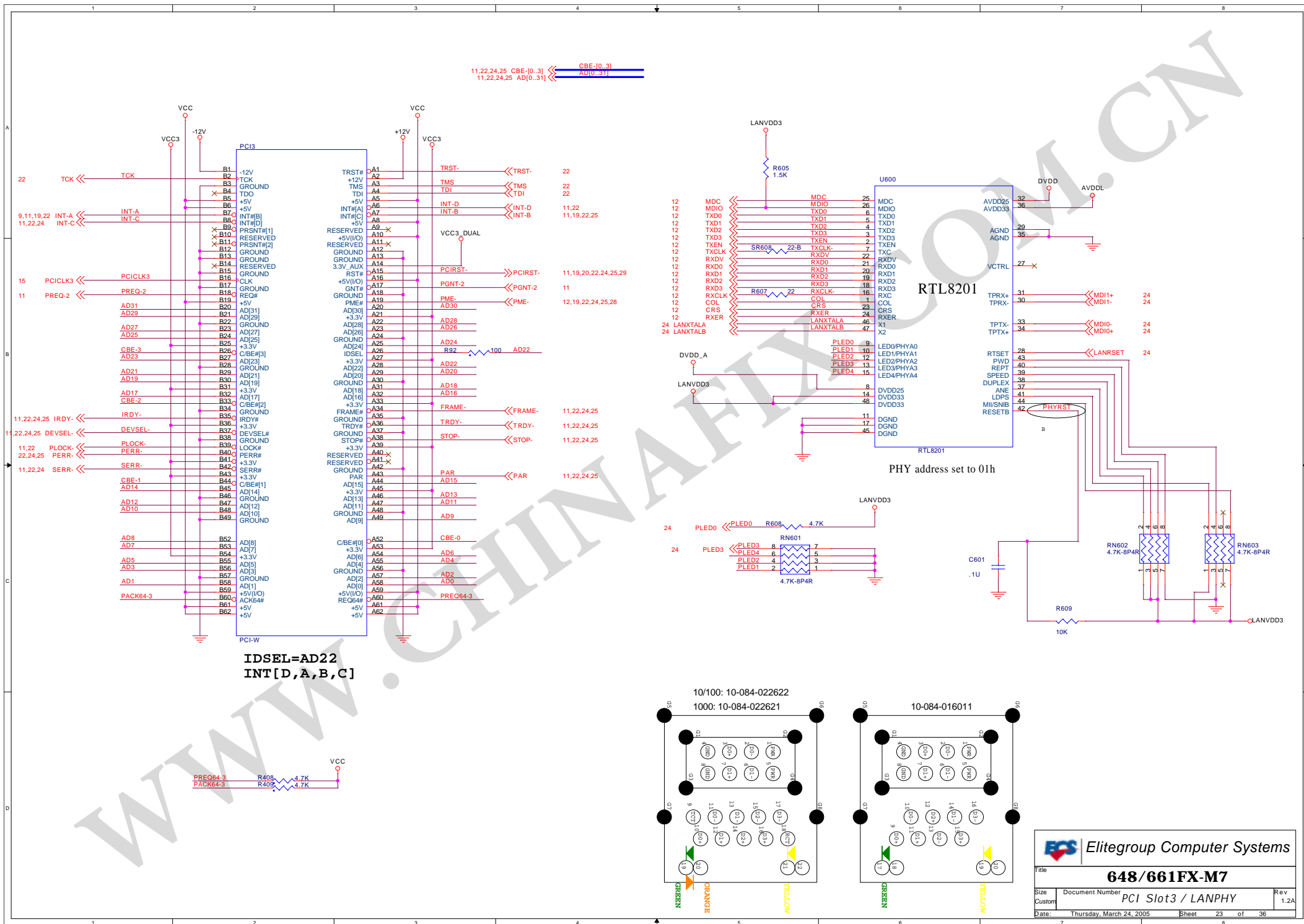
IDSEL=AD20
INT[B,C,D,A]

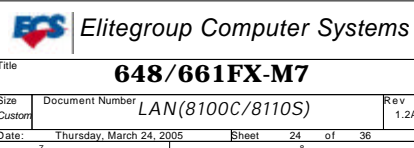


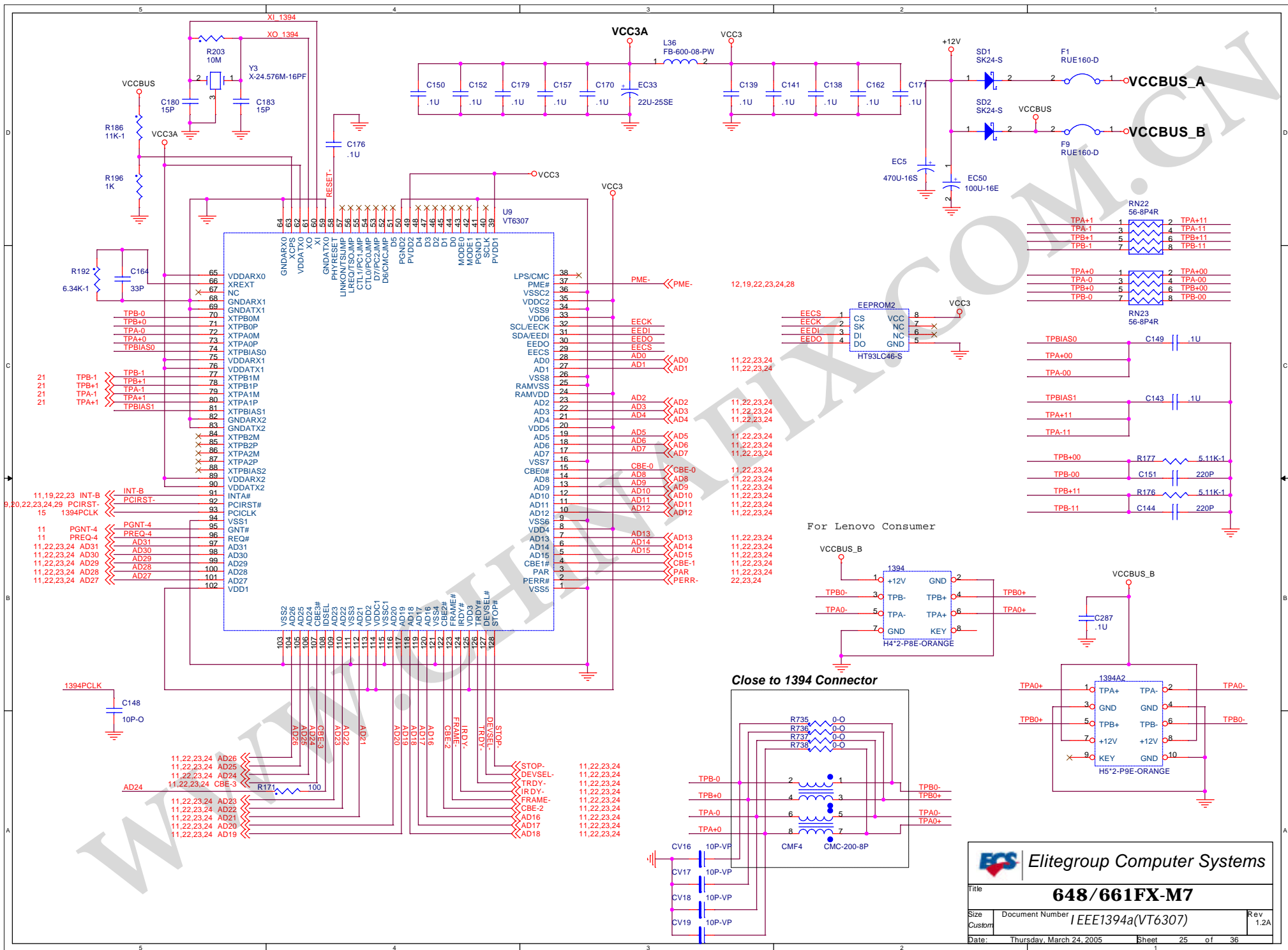
IDSEL=AD21
INT[C,D,A,B]

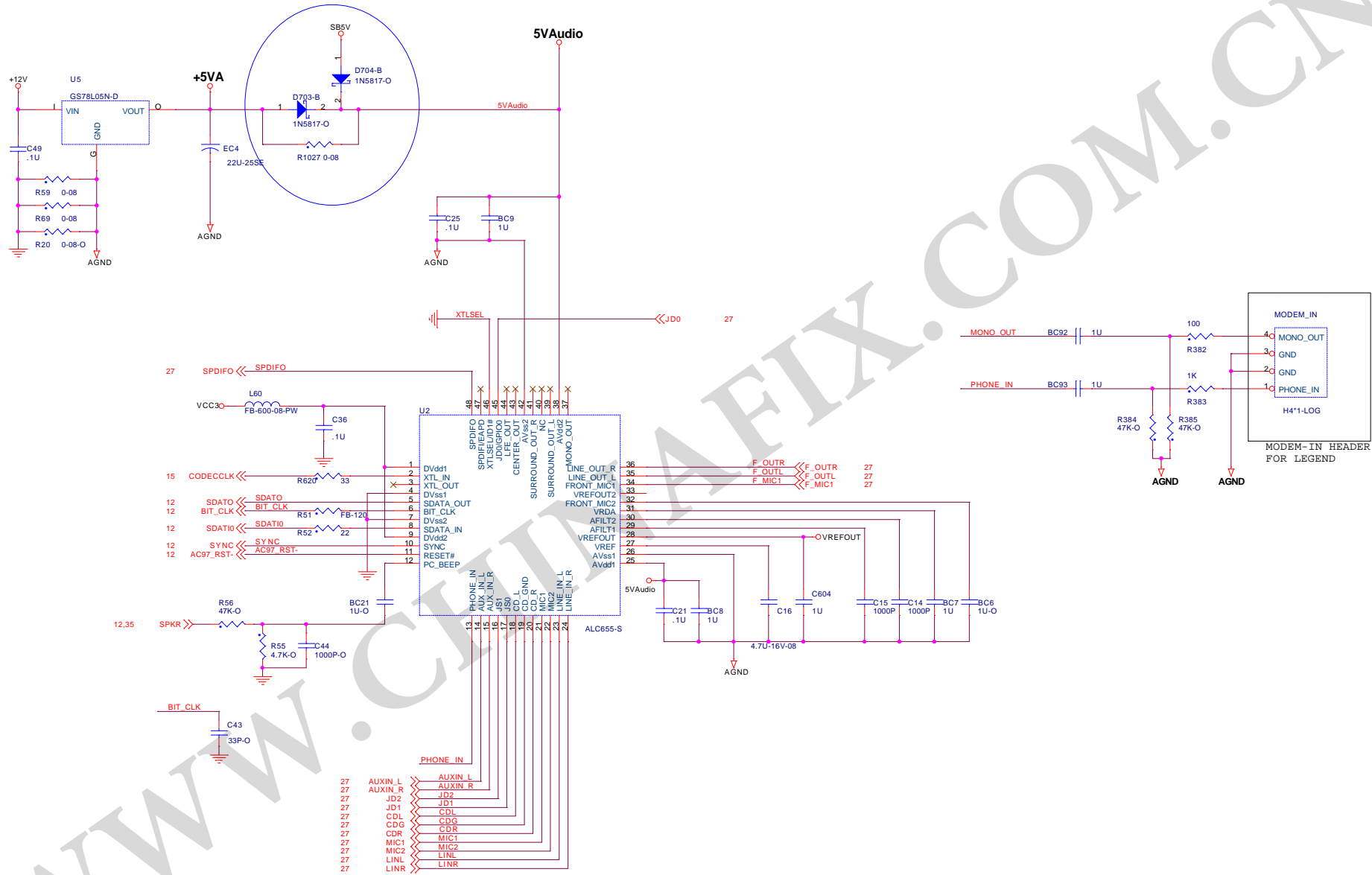


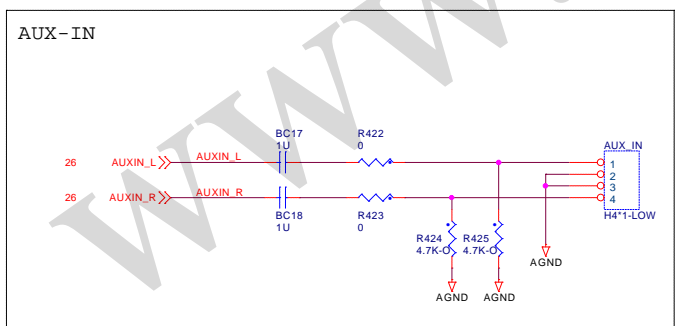
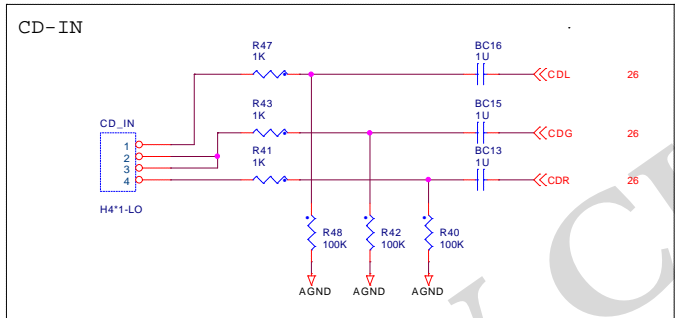
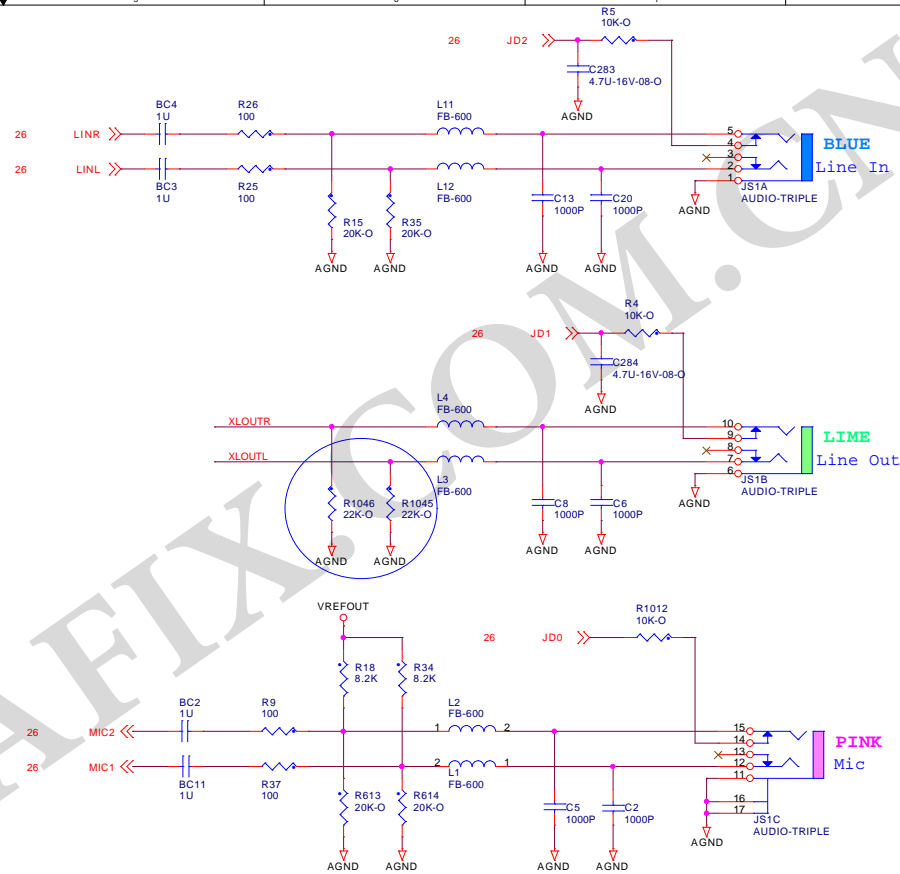
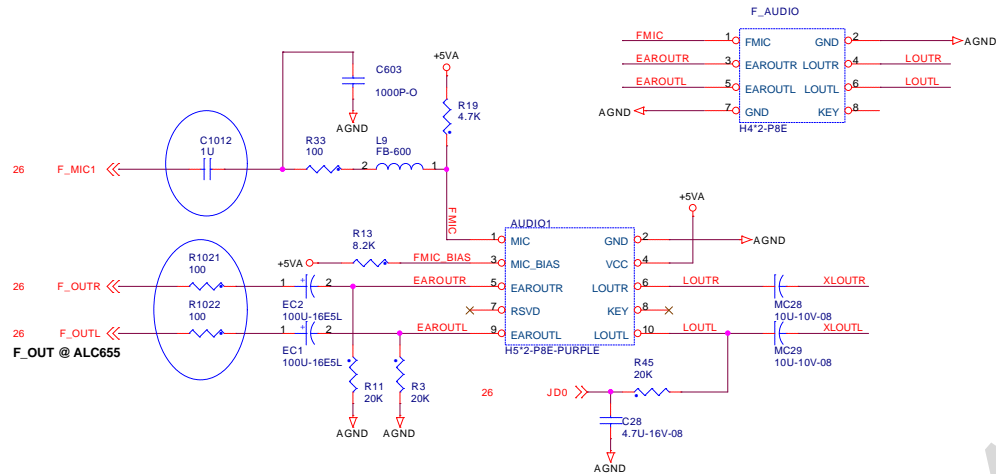
每個 PCI 插槽 pin A33
各放一顆





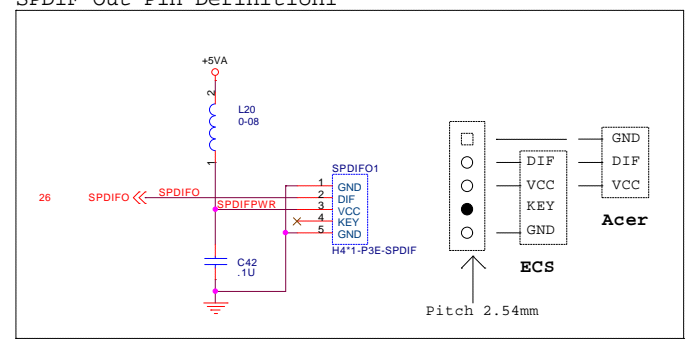




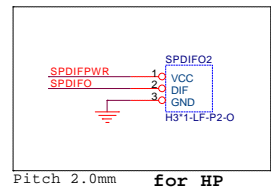


☐ ADD ACER 3-PIN SPEC

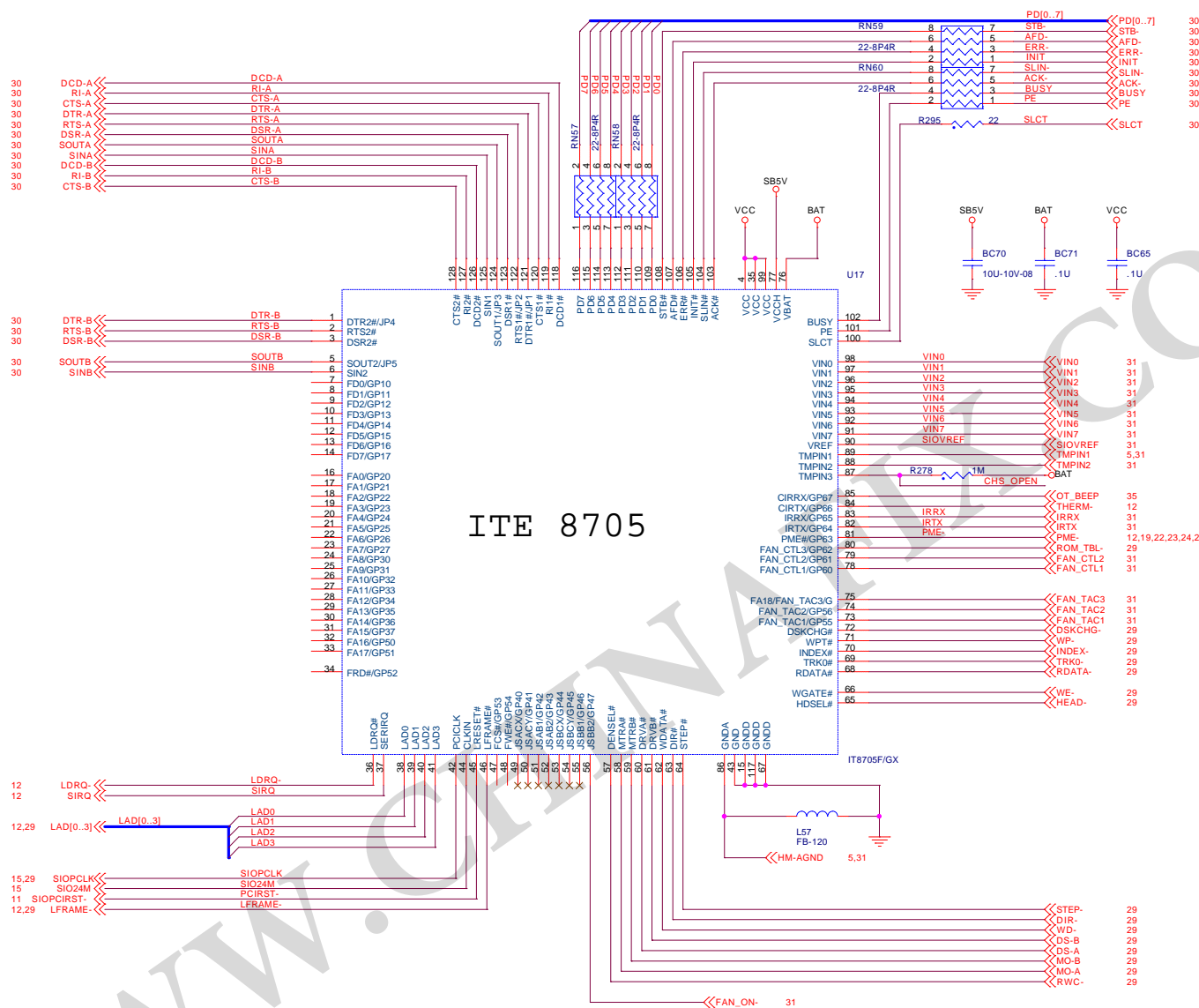
SPDIF-Out Pin Definition1



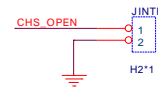
SPDIF-Out Pin Definition2



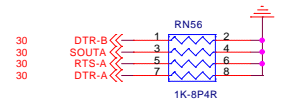
Pitch 2.0mm for HP



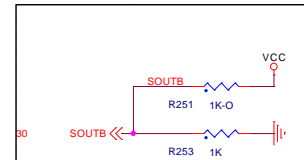
		High	Low
GPIO62	BootBlockProtect	Disable	Enable



ITE 8705 POWER ON TRAPS

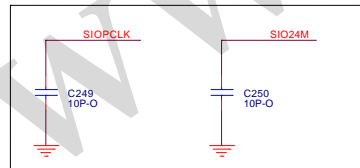


- 1.If use LPC ROM, pull down DTR#A RTS#A SOUTA DTR#B
- 2.If use Legacy 2MB flash rom, pull high DTR#A RTS#A SOUTA DTR#B
- 3.If use Legacy 4MB flash rom, pull high DTR#A RTS#A SOUTA DTR#B



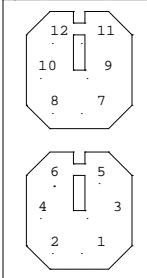
POWER ON TRAP

SOUTB
HIGH: 4M FLASH ROM ENABLE (PIN 75 IS FA18)
LOW : PIN 75 IS FAN_TAC3



Place near to ITE8705

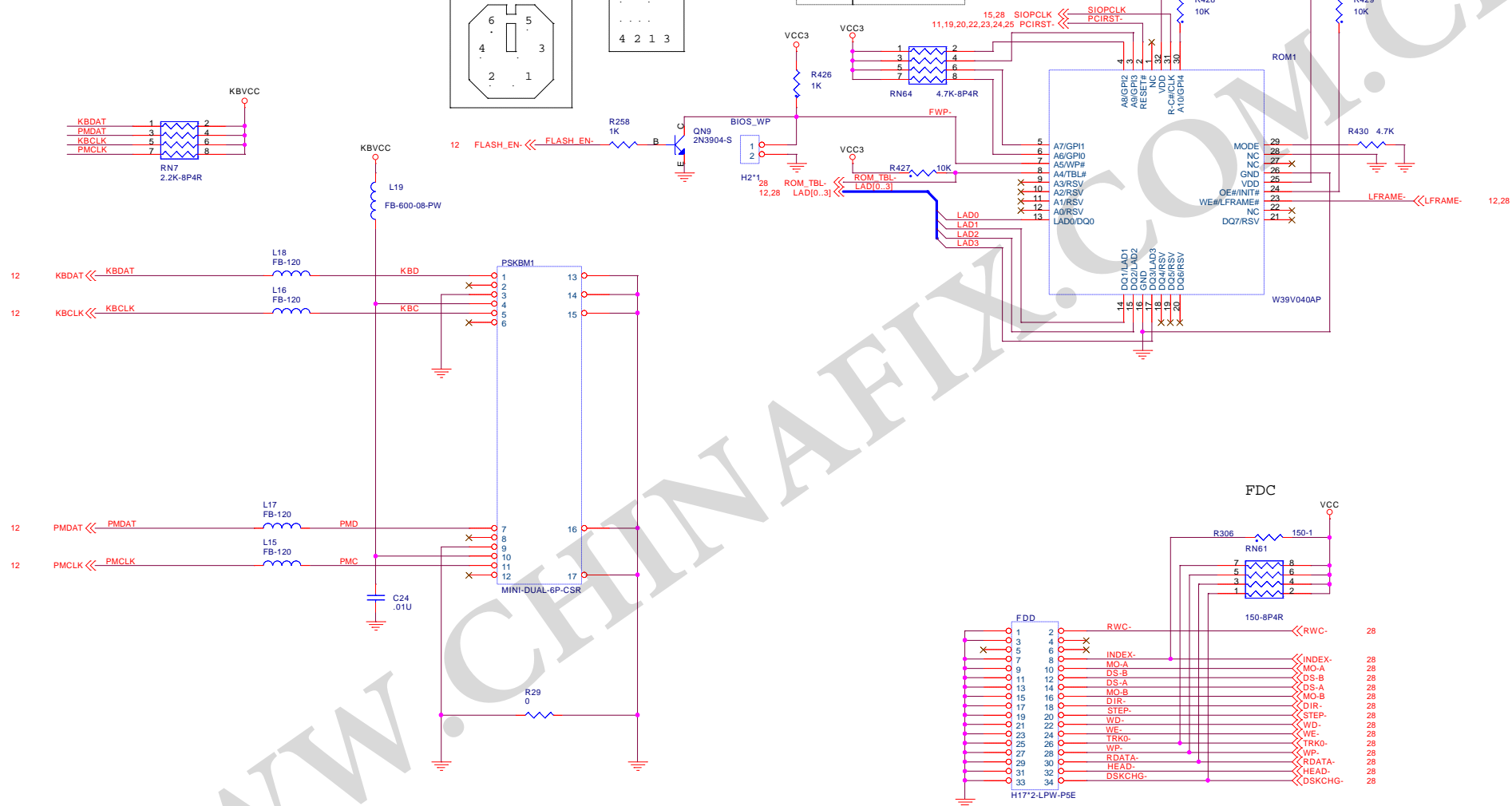
CONNECTOR VIEW



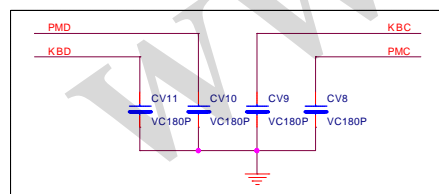
TOP VIEW



JP3	BIOS PROTECT
OPEN	DISABLE
SHORT	ENABLE

LPC INTERFACE
ROM

PLACE NEAR CONNECTOR



Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA .

4pin header: SQN703, R750=100ohm, R225=0ohm-0805

	NR1A/NR1B	RI#
<i>Normal</i>	-12V	<i>High</i>
<i>Active</i>	+12V	<i>Low</i>

WOM

1 2 3

H3*1-TWW-P2mm

WOL

1 1
2 2
3 3

H3*1-TWW-P2mm

[illegible]

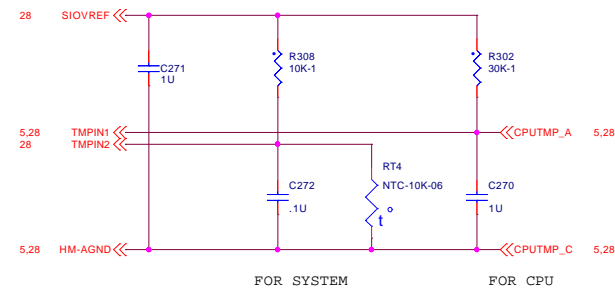
DEL D700


```
modify SQN702, SR740,SR741,SR742, R417-->SR417
```

Near to 8705 chip

The schematic diagram illustrates the IRDA interface circuit. A 12V GPIR pin is connected to a 10K resistor (R419) to ground and a 1K resistor (R420) to the IRRX pin of the H61-P3E module. The IRRX pin is also connected to a 1K resistor (R420) to VCC. The IRTX pin of the module is connected to ground. The module pins are labeled GPI, VCC, NC, IRRX, GND, and IRTX.

Choosing method of measuring temperature by
either thermistor or diode



		<i>Elitegroup Computer Systems</i>	
Title		648/661FX-M7	
Size Custom	Document Number <i>HM / FAN / RING</i>	Rev 1.2A	
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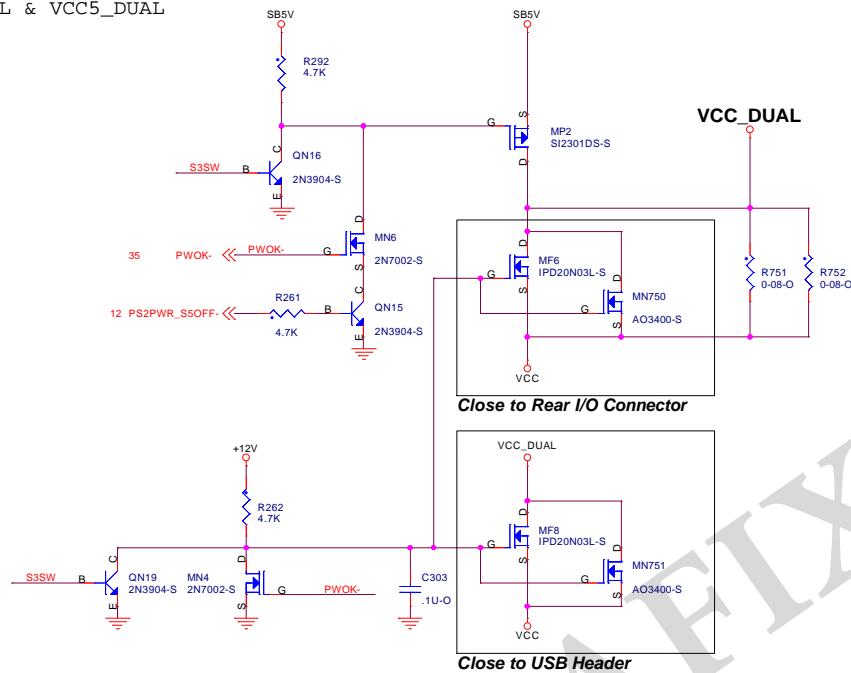
AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1. IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

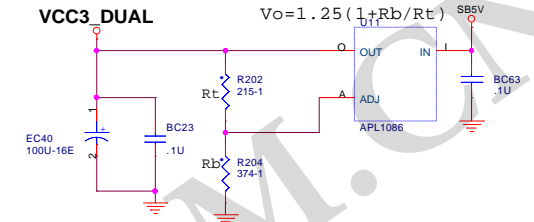
2. IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER.(ADDITIONAL
500mA PER USB PORT)

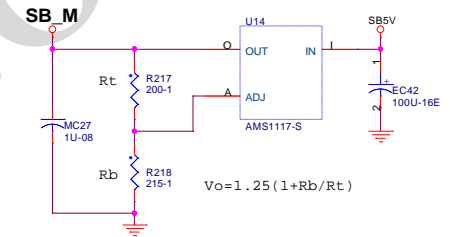
VCC3_DUAL & VCC5_DUAL



VCC3_DUAL

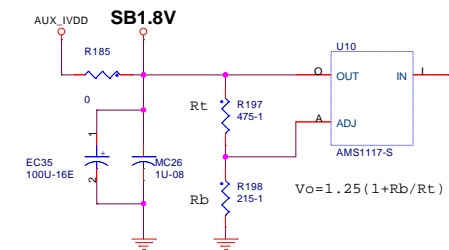


SB_M

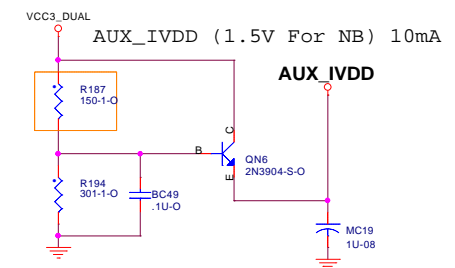


SB1.8V (For SB) 450mA

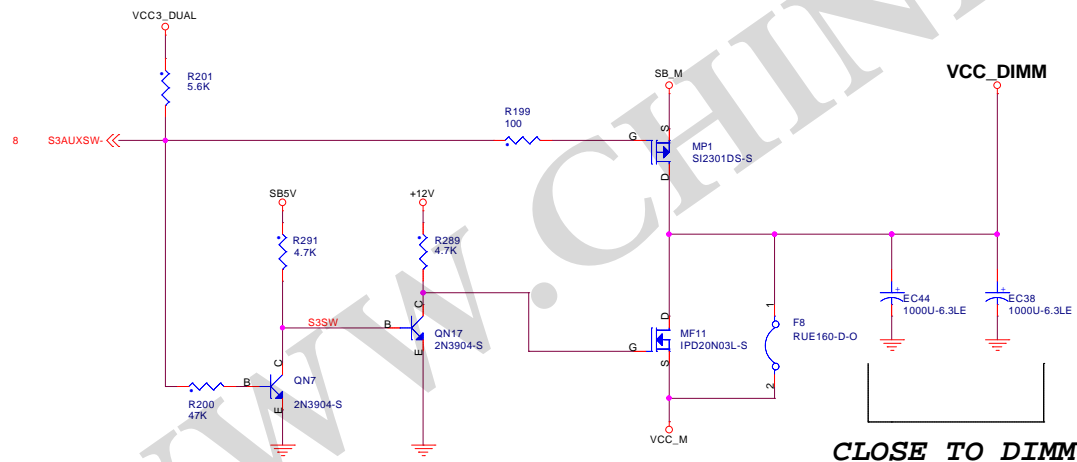
AUX_IVDD SB1.8V



VCC3_DUAL

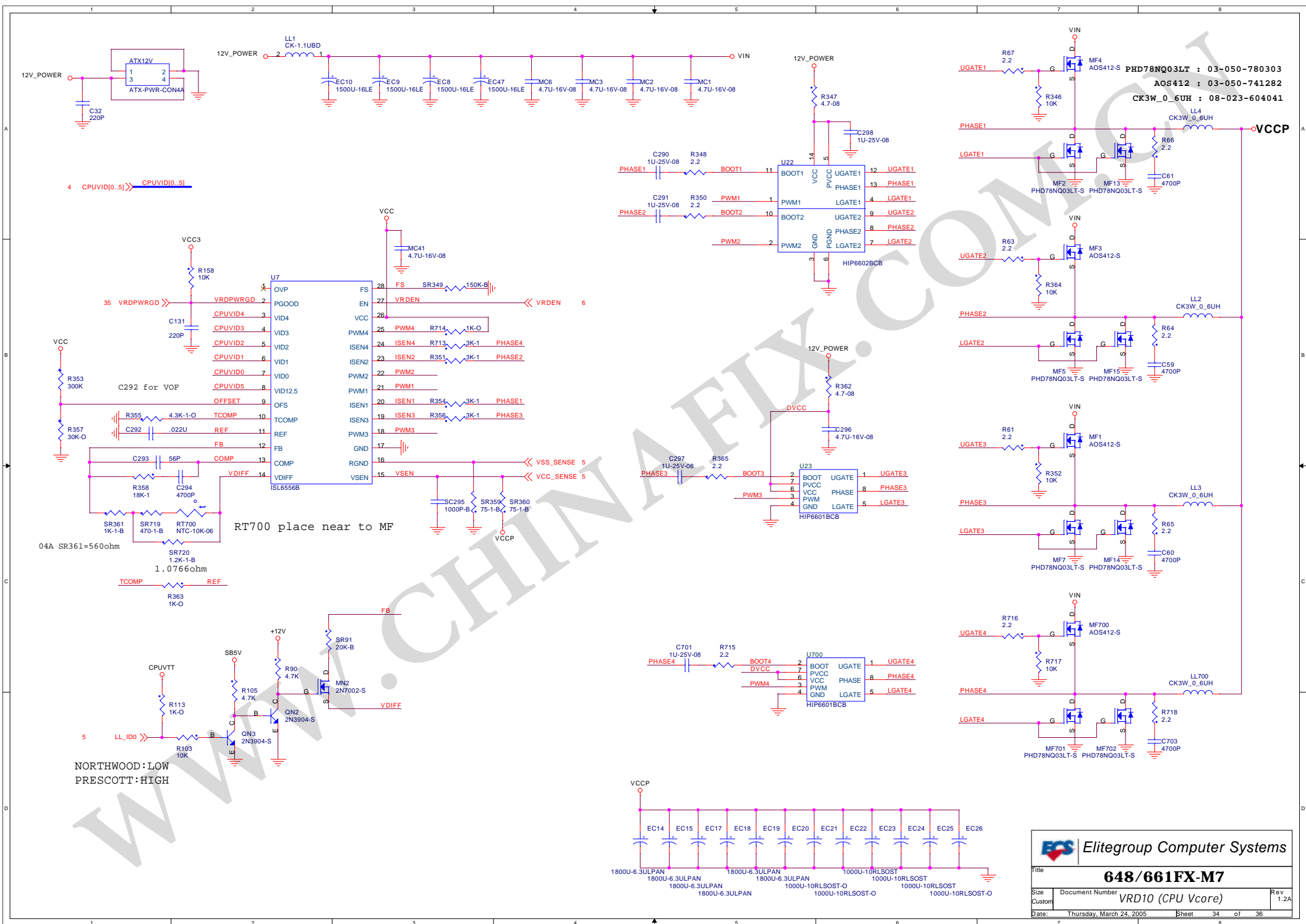


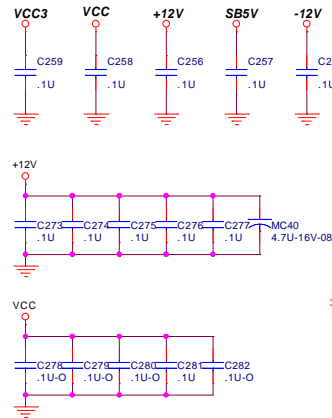
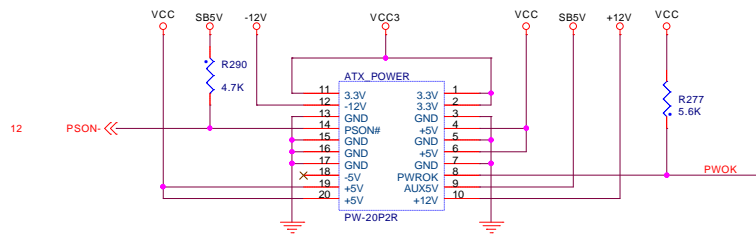
VCC3_DUAL



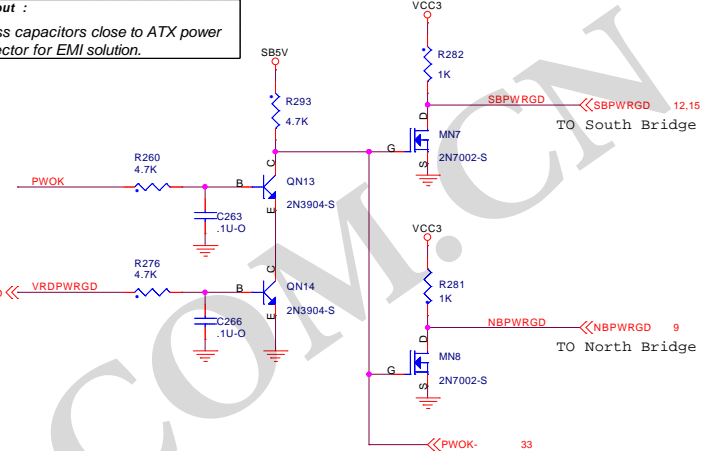
VCC_DIMM

CLOSE TO DIMM

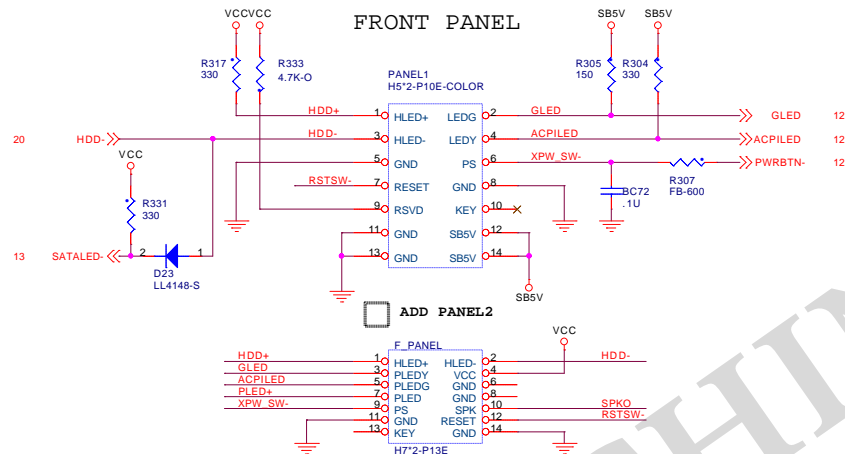




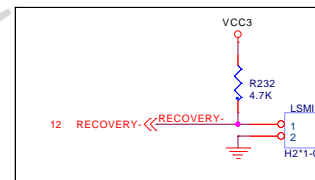
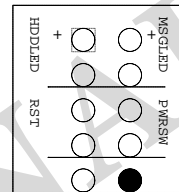
Layout :
Bypass capacitors close to ATX power connector for EMI solution.



Hardware Reset Circuit

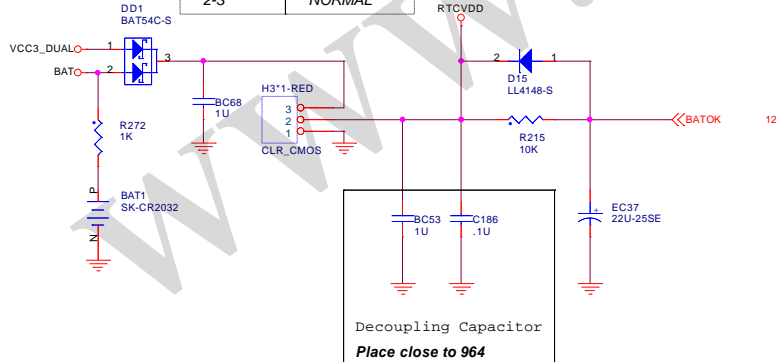


Intel Front Panel



For Acer

CLR_CMOS	CLEAR CMOS
1-2	CLEAR
2-3	NORMAL



NOTE!

- 1.The RTCVDD is 3V
 - 2.Decoupling capacitor must be close to 635 RTCVDD pin.
 - 3.RTC circuit must strictly follow SiS's recommended design.
- SiS is not responsible for RTC problems from foreign designs.

1. BOM Attention

(1) South Bridge

Option	SIS964	SIS964L
Components		
U13	964 964142	964L 964162
R241	374 374010	X
R71, R74	33 330000	X
R72, R75	49.9 499010	X
R331	330 330001	X
D23	1N4148 03-021-214890	X
SATA1, SATA2	10-020-007690	X

(3) On-Board VGA

Option	Support	No Support
Components		
U8	661FX 661141	648FX 648161
L30, L31, L32, L6, L7, L8	FB-120	X
C112, C116, C117, BC35	1U	X
C118, C119	.1U	X
MC36, MC37	10U	X
R136	130 130011	X
R134, R143	33	X
R128, R135	100	X
VGA1	10-717-015010	X
C111, C114, C115	22P	X
R22, R23, R24	75	X
R32, R39	2.2K	X
CV1~7	22P-VP 04-150-220003	X
F2	O	X

(3) LAN

Option	8100C 10/100 Mbps	8110S 1Gbps	8110SB 1Gbps	8201BL 10/100 Mbps	8201CL 10/100 Mbps
Components					
LAN1	RTL8100C 01-230-100351	RTL8110S 01-230-110350	RTL8110SB	RTL8201BL 02-448-201861	RTL8201CL 02-462-201860
R53	5.6K-1	2.49K-1	2.49K-1	5.9K-1	2K-1
R12, R14, R21, R28	X	49.9	X	X	X
C10, C18	X	0.1u	X	X	X
C52, C53, C54	X	0.01u	X	X	X
C51	0.1u	0.01u	0.01u	X	0.1u
RJ2	X	(1-2) 0 ohm	X	X	(2-3) 0 ohm
R604	X	X	X	X	0 ohm
C601	X	X	X	X	0.1u
L14/ C23	X	0 ohm/ 0.1u	0 ohm/ 0.1u	X	X
RJ7/ C19	(1-2)FB-600 /10u-08	X	(2-3)FB-600 /10u-08	X	X
L21	0 ohm	X	X	0 ohm	0 ohm
QP1	X	HA8550	HA8550	X	X
RJ1	(1-2) 0 ohm	(2-3) 0 ohm	(2-3) 0 ohm	X	X
RJ8	X	X	X	X	(2-3) 0 ohm
QP3	HPN2907A	HA8550	HA8550	X	X
RN601, RN602, RN603	X	X	X	4.7K-8P4R	4.7K-8P4R
C601	X	X	X	0.1u	0.1u
R608/ R609	X	X	X	4.7K/ 10K ohm	4.7K/ 10K ohm
R605	X	X	X	1.5K ohm	1.5K ohm
R602, R603, R607	X	X	X	22 ohm	22 ohm
SR600/ SR601/ SR602/ SR603/ SR607/ SR608	X	X	X	22 ohm-B	22 ohm-B
SR606	150 ohm-B	150 ohm-B	150 ohm-B	X	X
SR604/ SR605	15K/ 1K ohm-B	15K/ 1K ohm-B	15K/ 1K ohm-B	X	X
Y600/ R600	X	X	X	Y-25M/ 0 ohm	Y-25M/ 0 ohm
C166/ C600	4.7K ohm/ X	4.7K ohm/ X	4.7K ohm/ X	22P	22P
R190/ R191	X / 1K ohm	X / 1K ohm	X / 1K ohm	1K ohm/ X	1K ohm/ X
EEPROM1/ EEPROM3	O / X	O / X	O / X	X / O	X / O
R54/ R610	3.6K ohm/ X	3.6K ohm/ X	3.6K ohm/ X	X / 4.7K ohm	X / 4.7K ohm

2. GPIO Function

GPIO	Status	0	1	Jumper
GPIO5	* RESERVED	RESERVED	RESERVED	JP4
GPIO6	* RESERVED	RESERVED	RESERVED	JP5
GPIO7	* LAN Selection	LANPHY	PCILAN	N/A
GPIO9	USB, PS/2 S4/S5 Wake Up	Disable	Enable	N/A
GPIO10	DDR Voltage	2.54V	2.63V	N/A
GPIO11	* WHQL	No Support	Support	JPT3
GPIO13	Flash Write Protect	Un-Protect	Protect	

(1) "*" means that the function is selective and ECS may make changes at any time, without notice in this page.

(2) Jumper Setting (Header 3*1):

1: (1-2)

0: (2-3)

(3) Please see Page.12 for more detail jumper function.

JPT3	1-2	2-3
GPIO11	1	0
HP	Clear CMOS	Normal
TRIGEM	Suspen Mode	S1 & S3

JPT4	1-2	2-3
GPIO5	1	0
HP	Clear Password	Normal
TRIGEM	BIOS Logo	TG

